SNC7352x Series

32-bit Dual-Core Microcontroller

1 Introduction

1.1 Features

CPU

- Two ARM® Cortex®-M3 Processors (Core 0 and Core 1), each up to 162 MHz
- One serial wire debug (SWD) port
- Built-in Memory Protect Unit (MPU)
- Built-in Nested Vectored Interrupt Controller (NVIC)
- One interrupt signal for the interaction between the two cores
- System clocks
  – High: 12 MHz XTAL and IHRC at 1.2V
  – Low: ILRC at 1.2V
- Supports fast Fourier transform (FFT)/finite impulse response (FIR) accelerator (Core 1)

Memory

- Internal memory
  – ROM size for Core 0: 64 KB
  – PRAM size for Core 0: 64 KB
  – ROM size for Core 1: 128 KB
  – Shared AHB SRAM: 256 KB
  – Shared Mailbox RAM: 4 KB
- SPI NOR flash controller
  – Clock frequency: Up to 40.5 MHz
  – Size: Up to 256 MB
  – Supports 1/2/4-bit mode
  – Supports execute in place (XIP)
- DRAM controller
  – 4 channels with burst transfer
  – Supports OPI PSRAM
- Supports one 16 KB I-cache
- DMA controllers with 19 channels
- Storage
  – SD card controller (SD0)
  – NAND flash controller with 8-bit ECC

System Control (Core 0)

- Power Management Unit (PMU)
  – Operation modes: Normal/sleep/deep sleep/deep power-down (DPD)
  – DPD with optional wakeup pin
- Low Voltage Reset (LVR)
  – 0.8V or 0.95V for core
  – 1.8V for I/O (power-on/power-off)
  – 2.1V for I/O (normal mode)
- ROM/RAM remap

Peripherals

- Up to 80 general-purpose input/output (GPIO) pins
- Up to three master/slave Inter-Integrated Circuit (I^2C) buses
- Serial Peripheral Interface (SPI) controller
- Up to two Universal Asynchronous Receivers/Transmitters (UART)
- Up to eight timers/counters with 32-bit prescale counter (CT32B) providing 24 PWM outputs
- Two 8-bit Watchdog timers (WDT)
- 10-bit SAR ADC with up to six input channels
- SD/SDIO controller (SD1)
- SPI controllers with DMA
  – Supports one-byte FIFO
  – Supports 1/2/4-bit DMA mode
  – With 8-bit Error Correcting Code (ECC)
- USB 2.0 high speed host
  – Supports MSC/HUB/UVC class
  – Supports accelerator for ISO transfer
- USB 2.0 high speed host/device
  – Supports MSC/HID/UAC/UVC class
  – Host/device option

Multimedia

- CMOS Image Sensor (CIS) interface
  – Supports resolution in VGA/CIF/QVGA/ QCIF/QQVGA
  – Supports scaling and windowing
  – Supports Line to block (L2B) mode
- Color Space Converter (CSC)
- JPEG 422/420 codec
- TFT-LCD interface
  – Supports resolution of up to 480 x 272
  – 8-bit serial RGB and 18-bit parallel RGB
  – UPS051 (serial RGB)/UPS052 (serial dummy RGB)
  – RGB565 format only
- 8/16-bit 8080 MCU interface
- Up to five I^2S interfaces
  – Communicates in master or slave mode
  – Connects to audio codecs in slave mode only
  – Left/right justified format

Voltage

- Core: 1.2V typically
- I/O: 3.3V typically
- DRAM: 1.8V typically

Package

- LQFP80L
- LQFP128L

1.2 Application

The applications of the SNC7352x series include:

- Touch LCD
- Toy cameras
- Educational products
- Home automation

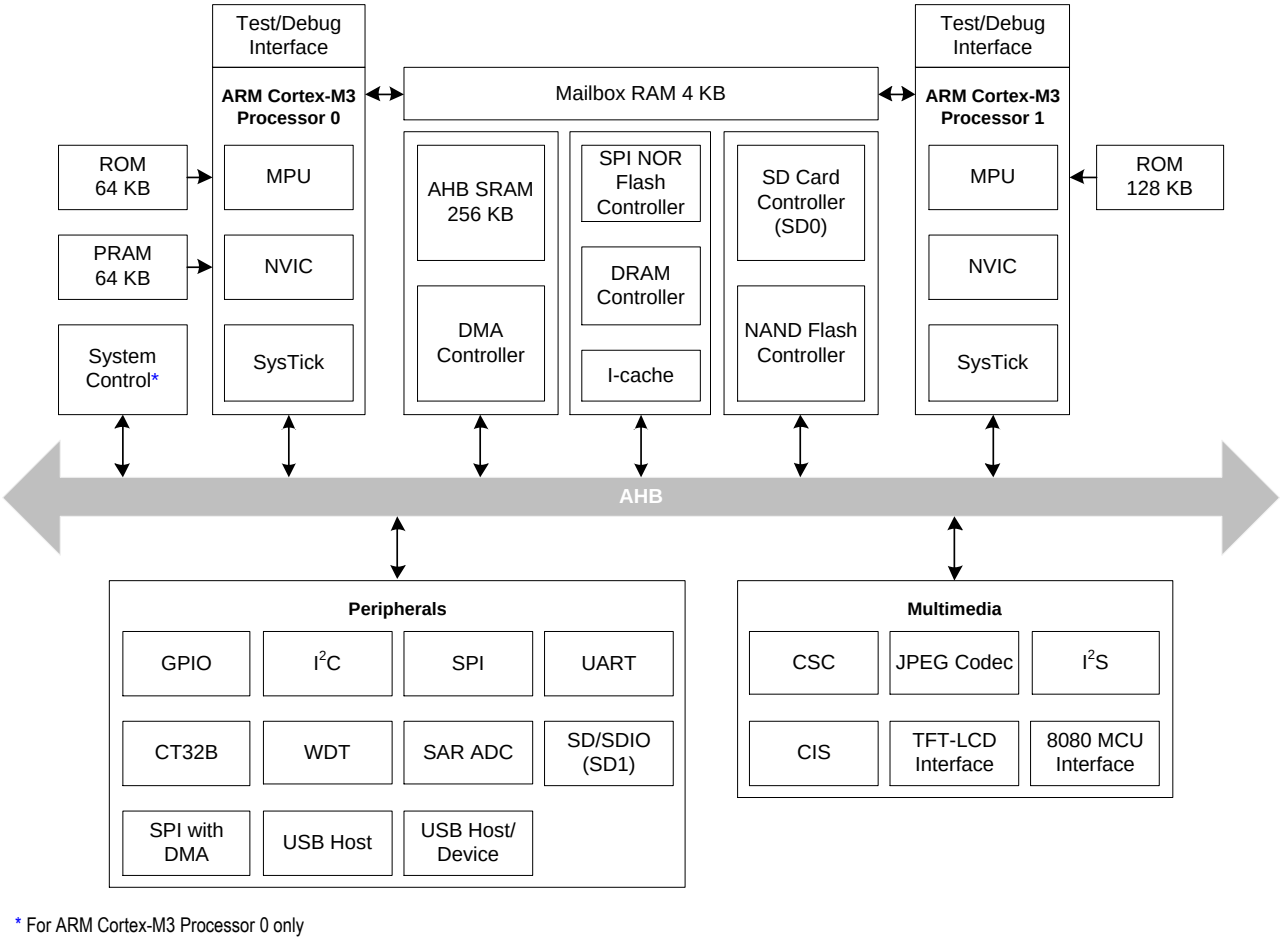
1.3 Description

The SNC7352x series is a highly-integrated microcontroller with two 32-bit ARM Cortex-M3 processors in symmetric dual-core architecture. Each of the two cores controls respective designated peripherals, cooperates with the other, and can be independently programmed. The two cores operate at a frequency of up to 162 MHz individually. Supporting RAM array with data bandwidth of up to 5 GB/sec and deep power-down mode consuming less than 1 μA, the SNC7352x series is a suitable solution for the LCD application.

Standard peripherals of the SNC7352x series include GPIO, I^2C, SPI, UART, CT32B, WDT, SAR ADC, SD/SDIO, SPI with DMA, SPI NOR flash controller, NAND flash controller, USB, and I^2S, providing extensive connectivity with the external devices. Equipped with a TFT-LCD interface and an 8080 MCU interface, the SNC7352x series supports seamless communication with LCD panels. The CMOS image sensor interface enables the SNC7352x series to capture images, and the Color Space Converter and JPEG codec ensure efficient conversion and compression of the image data.

The SNC7352x series is backed by comprehensive software support and tools. A wide range of libraries not only allows easy programming and debugging but also features image compilation and animation, offering flexibility in designs. Incorporating two Cortex-M3 cores, power management unit, and various peripherals, the SNC7352x series, along with the image processing functions, delivers the performance necessary for a variety of LCD applications.

1.4 Functional Block Diagram



* For ARM Cortex-M3 Processor 0 only

Figure 1–1 Functional Block Diagram

1.5 Support

Sonix offers an extensive line of tools available for the SNC7352x series including a software development kit (SDK) with RTOS based development environment and other useful development tools such as:

- Mass production test tool
- Firmware download tool

For information on pricing and availability, please contact the nearest Sonix sales office or an authorized distributor.

Revision History

Date	Revision	Description
24-Jul-2023	1.0	Initial release
30-Aug-2023	1.1	Added SNC73522 and all related information Updated Device Operating Conditions
13-Dec-2023	1.2	Updated Absolute Maximum Ratings

Convention

ⓘ **WARNING**	Indicates a hazard with a medium or low level of risk that, if not avoided, could result in minor or moderate injury.
🛠 **TIP**	Indicates a tip that may help you solve a problem or save time.
🕮 **NOTE**	Provides additional information to emphasize or supplement important points of the main text.

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2 Device Comparison

Device	Package	SiP Memory	USB Host	USB Device/ Host	I/O	I²C	UART	PWM	SAR ADC	SD/ SDIO	SPI DMA	SD Card	NAND	I²S	CIS	LCD
SNC73520	LQFP80L	–	–	✓	58	2	1	17	4-CH	✓	2	✓	–	3	✓	8-bit 8080/RGB
SNC73521		8 MB OPI PSRAM														
SNC73522	LQFP128L	8 MB OPI PSRAM	✓	✓	80	3	2	24	6-CH	✓	2	✓	✓	5	✓	8/16-bit 8080/ 18-bit RGB

3 Pin Information

3.1 SNC73520

3.1.1 Pin Diagram

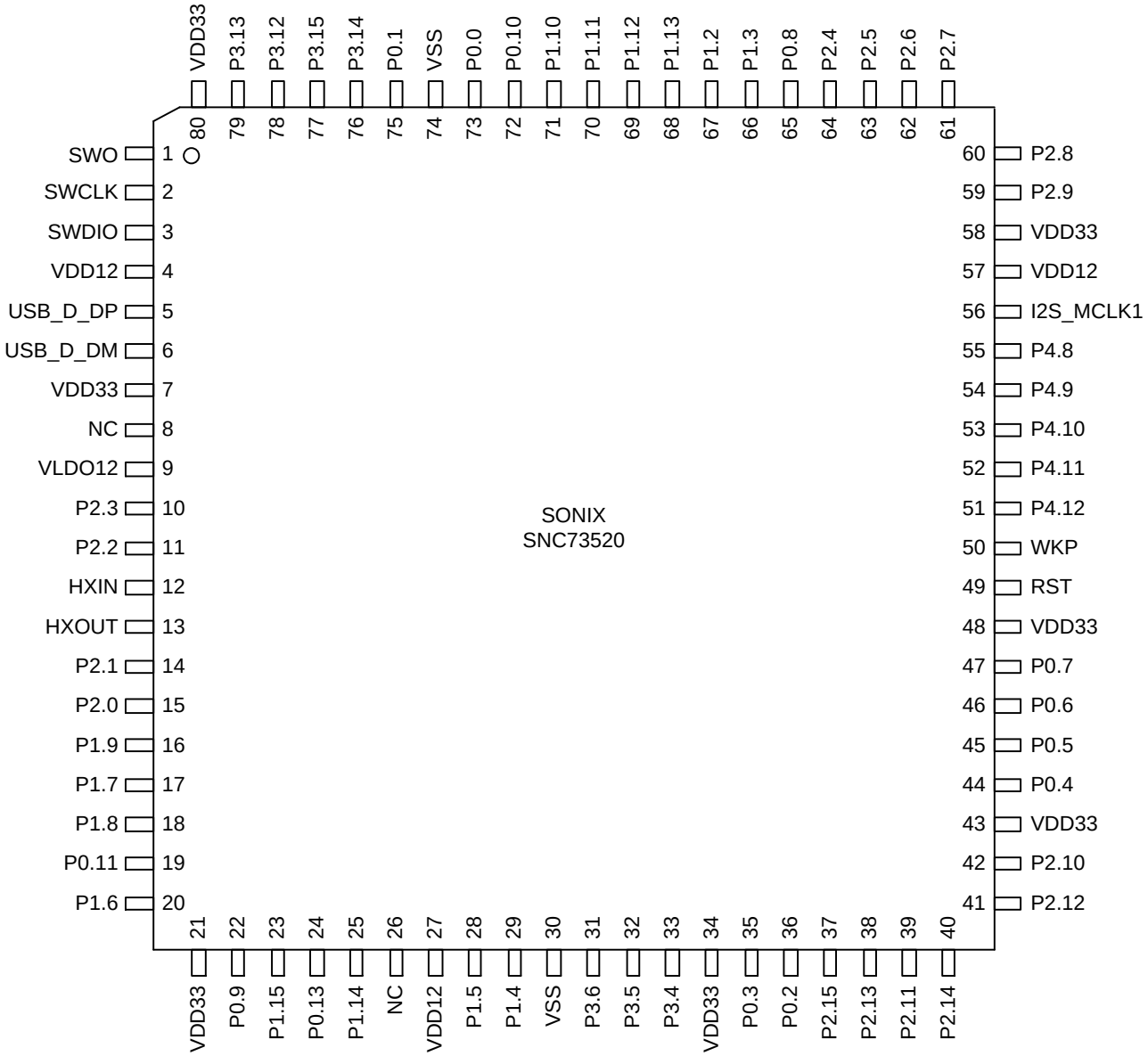


Figure 3–1 SNC73520 Pin Diagram

3.1.2 Pin Description

Table 3–1 SNC73520 Pin Description

No.	Name	Type[1]	Mode[2]	Description
1	SWO	O	D	Serial wire output trace port
	P4.5	I/O	1	GPIO4 pin 5
	CT32B0_PWM2	O	7	32-bit timer/counter 0 pulse width modulation data output 2
2	SWCLK	O	D	Serial wire clock
	P4.6	I/O	1	GPIO4 pin 6
	CT32B0_PWM1	O	7	32-bit timer/counter 0 pulse width modulation data output 1
3	SWDIO	I/O	D	Serial wire debug bi-directional data. A pull-up resistor, 100 kΩ recommended by ARM, is required.
	P4.7	I/O	1	GPIO4 pin 7
	CT32B0_PWM0	O	7	32-bit timer/counter 0 pulse width modulation data output 0
4	VDD12	P	–	1.2V power supply
5	USB_D_DP	A I/O	–	USB D+ signal
6	USB_D_DM	A I/O	–	USB D- signal
7	VDD33	P	–	3.3V power supply
8	NC	–	–	Not connected
9	VLDO12	P	–	Internal 1.2V LDO output
10	P2.3	I/O	D	GPIO2 pin 3
	SDIO_D3	I/O	1	SD/SDIO (SD1) data
11	P2.2	I/O	D	GPIO2 pin 2
	SDIO_D2	I/O	1	SD/SDIO (SD1) data
	I2S4_WS	I/O	5	I²S4 word select
12	HXIN	I	–	External 12 MHz crystal input
13	HXOUT	O	–	External 12 MHz crystal output
14	P2.1	I/O	D	GPIO2 pin 1
	SDIO_D1	I/O	1	SD/SDIO (SD1) data
	I2S4_BCLK	I/O	5	I²S4 bit clock. Bit clock can be programmed as a master or a slave.
15	P2.0	I/O	D	GPIO2 pin 0
	SDIO_D0	I/O	1	SD/SDIO (SD1) data
	I2S4_DOUT	O	5	I²S4 data output
16	P1.9	I/O	D	GPIO1 pin 9
	SD0_D3	I/O	1	SD0 data
	CIS_D3	I	2	CMOS image sensor output data
	LCD_D3/ 8080_D3	O	4	TFT-LCD data bus/ 8080 CPU data bus
	SPI0DMA_MISO3	I	5	SPI0 with DMA master in slave out
	CT32B6_PWM0	O	7	32-bit timer/counter 6 pulse width modulation data output 0
17	P1.7	I/O	D	GPIO1 pin 7
	SD0_D1	I/O	1	SD0 data
	CIS_D1	I	2	CMOS image sensor output data
	LCD_D1/ 8080_D1	O	4	TFT-LCD data bus/ 8080 CPU data bus
	SPI0DMA_MOSI	O	5	SPI0 with DMA master out slave in
	CT32B6_PWM2	O	7	32-bit timer/counter 6 pulse width modulation data output 2
18	P1.8	I/O	D	GPIO1 pin 8
	SD0_D2	I/O	1	SD0 data
	CIS_D2	I	2	CMOS image sensor output data
	LCD_D2/ 8080_D2	O	4	TFT-LCD data bus/ 8080 CPU data bus
	SPI0DMA_MISO2	I	5	SPI0 with DMA master in slave out
	CT32B6_PWM1	O	7	32-bit timer/counter 6 pulse width modulation data output 1

[1] Signal Types:
I = Input
O = Output
A = Analog signal
P = Power
GND = Ground

[2] D = Default

No.	Name	Type[1]	Mode[2]	Description
19	P0.11	I/O	D	GPIO0 pin 11
	SPIFC_MOSI	O	1	SPI NOR flash master out slave in
	SPI0DMA_MOSI	O	3	SPI0 with DMA master out slave in
20	P1.6	I/O	D	GPIO1 pin 6
	SD0_D0	I/O	1	SD0 data
	CIS_D0	I	2	CMOS image sensor output data
	LCD_D0/ 8080_D0	O	4	TFT-LCD data bus/ 8080 CPU data bus
	SPI0DMA_MISO	I	5	SPI0 with DMA master in slave out
	CT32B7_PWM0	O	7	32-bit timer/counter 7 pulse width modulation data output 0
21	VDD33	P	–	3.3V power supply
22	P0.9	I/O	D	GPIO0 pin 9
	SPIFC_CLK	O	1	SPI NOR flash clock output
	SPI0DMA_SCLK	O	3	SPI0 with DMA serial clock
23	P1.15	I/O	D	GPIO1 pin 15
	SDIO_CMD	O	1	SD/SDIO (SD1) command
	I2S4_DIN	I	5	I²S4 data input
24	P0.13	I/O	D	GPIO0 pin 13
	CT32B0_PWM0	O	7	32-bit timer/counter 0 pulse width modulation data output 0
25	P1.14	I/O	D	GPIO1 pin 14
	SDIO_CLK	O	1	SD/SDIO (SD1) clock output
	I2S4_MCLK	I/O	5	I²S4 master clock
26	NC	–	–	Not connected
27	VDD12	P	–	1.2V power supply
28	P1.5	I/O	D	GPIO1 pin 5
	SD0_CMD	O	1	SD0 command
	CIS_PCLK	I	2	CMOS image sensor pixel clock
	LCD_DCLK/ 8080_A0	O	4	TFT-LCD clock/ 8080 CPU address 0
	SPI0DMA_SCLK	O	5	SPI0 with DMA serial clock
	CT32B7_PWM1	O	7	32-bit timer/counter 7 pulse width modulation data output 1
29	P1.4	I/O	D	GPIO1 pin 4
	SD0_CLK	O	1	SD0 clock output
	CIS_MCLK	O	2	CMOS image sensor master clock
	LCD_DE/ 8080_CS	O	4	TFT-LCD data enable/ 8080 CPU chip select; active low
	SPI0DMA_CS	O	5	SPI0 with DMA chip select
	CT32B7_PWM2	O	7	32-bit timer/counter 7 pulse width modulation data output 2
30	VSS	GND	–	Ground
31	P3.6	I/O	D	GPIO3 pin 6
	I2S1_WS	I/O	6	I²S1 word select
32	P3.5	I/O	D	GPIO3 pin 5
	I2S1_BCLK	I/O	6	I²S1 bit clock. Bit clock can be programmed as a master or a slave.
33	P3.4	I/O	D	GPIO3 pin 4
	I2S1_DIN	I	6	I²S1 data input
34	VDD33	P	–	3.3V power supply
35	P0.3	I/O	D	GPIO0 pin 3
	UART0_RXD	I	1	UART0 serial receive data
	CT32B7_PWM1	O	7	32-bit timer/counter 7 pulse width modulation data output 1
36	P0.2	I/O	D	GPIO0 pin 2
	UART0_TXD	O	1	UART0 serial transmit data
	CT32B7_PWM2	O	7	32-bit timer/counter 7 pulse width modulation data output 2
37	P2.15	I/O	D	GPIO2 pin 15
	LCD_D7	O	1	TFT-LCD data bus
	8080_D7	O	2	8080 CPU data bus
38	P2.13	I/O	D	GPIO2 pin 13
	LCD_D5	O	1	TFT-LCD data bus
	8080_D5	O	2	8080 CPU data bus
39	P2.11	I/O	D	GPIO2 pin 11
	LCD_D3	O	1	TFT-LCD data bus
	8080_D3	O	2	8080 CPU data bus

No.	Name	Type[1]	Mode[2]	Description
40	P2.14	I/O	D	GPIO2 pin 14
	LCD_D6	O	1	TFT-LCD data bus
	8080_D6	O	2	8080 CPU data bus
41	P2.12	I/O	D	GPIO2 pin 12
	LCD_D4	O	1	TFT-LCD data bus
	8080_D4	O	2	8080 CPU data bus
42	P2.10	I/O	D	GPIO2 pin 10
	LCD_D2	O	1	TFT-LCD data bus
	8080_D2	O	2	8080 CPU data bus
43	VDD33	P	–	3.3V power supply
44	P0.4	I/O	D	GPIO0 pin 4
	AIN0	I	1	ADC input channel 0
	CT32B7_PWM0	O	7	32-bit timer/counter 7 pulse width modulation data output 0
45	P0.5	I/O	D	GPIO0 pin 5
	AIN1	I	1	ADC input channel 1
	CT32B6_PWM2	O	7	32-bit timer/counter 6 pulse width modulation data output 2
46	P0.6	I/O	D	GPIO0 pin 6
	AIN2	I	1	ADC input channel 2
	CT32B6_PWM1	O	7	32-bit timer/counter 6 pulse width modulation data output 1
47	P0.7	I/O	D	GPIO0 pin 7
	AIN3	I	1	ADC input channel 3
	CT32B6_PWM0	O	7	32-bit timer/counter 6 pulse width modulation data output 0
48	VDD33	P	–	3.3V power supply
49	RST	I	–	Reset pin
50	WKP	I	–	Wakeup pin
51	P4.12	I/O	D	GPIO4 pin 12
	I2S0_WS	I/O	1	I²S0 word select
52	P4.11	I/O	D	GPIO4 pin 11
	I2S0_BCLK	I/O	1	I²S0 bit clock. Bit clock can be programmed as a master or a slave.
	CT32B2_PWM2	O	7	32-bit timer/counter 2 pulse width modulation data output 2
53	P4.10	I/O	D	GPIO4 pin 10
	I2S0_DIN	I	1	I²S0 data input
	CT32B3_PWM0	O	7	32-bit timer/counter 3 pulse width modulation data output 0
54	P4.9	I/O	D	GPIO4 pin 9
	I2C1_SDA	I/O	1	I²C1 serial data
	CT32B3_PWM1	O	7	32-bit timer/counter 3 pulse width modulation data output 1
55	P4.8	I/O	D	GPIO4 pin 8
	I2C1_SCL	O	1	I²C1 serial clock
	CT32B3_PWM2	O	7	32-bit timer/counter 3 pulse width modulation data output 2
56	I2S_MCLK1	O	–	I²S master clock output 1
57	VDD12	P	–	1.2V power supply
58	VDD33	P	–	3.3V power supply
59	P2.9	I/O	D	GPIO2 pin 9
	LCD_D1	O	1	TFT-LCD data bus
	8080_D1	O	2	8080 CPU data bus
60	P2.8	I/O	D	GPIO2 pin 8
	LCD_D0	O	1	TFT-LCD data bus
	8080_D0	O	2	8080 CPU data bus
	I2S4_WS	I/O	5	I²S4 word select
61	P2.7	I/O	D	GPIO2 pin 7
	LCD_DCLK	O	1	TFT-LCD clock
	8080_A0	O	2	8080 CPU address 0
	I2S4_BCLK	I/O	5	I²S4 bit clock. Bit clock can be programmed as a master or a slave.
	CT32B4_PWM2	O	7	32-bit timer/counter 4 pulse width modulation data output 2
62	P2.6	I/O	D	GPIO2 pin 6
	LCD_DE	O	1	TFT-LCD data enable
	8080_CS	O	2	8080 CPU chip select; active low
	I2S4_DOUT	O	5	I²S4 data output
	CT32B5_PWM0	O	7	32-bit timer/counter 5 pulse width modulation data output 0

No.	Name	Type[1]	Mode[2]	Description
63	P2.5	I/O	D	GPIO2 pin 5
	LCD_VSYNC	O	1	TFT-LCD vertical/frame synchronization
	8080_WR	O	2	8080 CPU write; active low
	I2S4_DIN	I	5	I²S4 data input
	CT32B5_PWM1	O	7	32-bit timer/counter 5 pulse width modulation data output 1
64	P2.4	I/O	D	GPIO2 pin 4
	LCD_HSYNC	O	1	TFT-LCD horizontal/line synchronization
	8080_RD	O	2	8080 CPU read; active low
	I2S4_MCLK	I/O	5	I²S4 master clock
	CT32B5_PWM2	O	7	32-bit timer/counter 5 pulse width modulation data output 2
65	P0.8	I/O	D	GPIO0 pin 8
	SPIFC_CS	O	1	SPI NOR flash chip select
	SPI0DMA_CS	O	3	SPI0 with DMA chip select
66	P1.3	I/O	D	GPIO1 pin 3
	CIS_HSYNC	I	2	CMOS image sensor output horizontal sync
	LCD_VSYNC/ 8080_WR	O	4	TFT-LCD vertical/frame synchronization/ 8080 CPU write; active low
67	P1.2	I/O	D	GPIO1 pin 2
	CIS_VSYNC	I	2	CMOS image sensor output vertical sync
	LCD_HSYNC/ 8080_RD	O	4	TFT-LCD horizontal/line synchronization/ 8080 CPU read; active low
68	P1.13	I/O	D	GPIO1 pin 13
	CIS_D7	I	2	CMOS image sensor output data
	LCD_D7/ 8080_D7	O	4	TFT-LCD data bus/ 8080 CPU data bus
69	P1.12	I/O	D	GPIO1 pin 12
	CIS_D6	I	2	CMOS image sensor output data
	LCD_D6/ 8080_D6	O	4	TFT-LCD data bus/ 8080 CPU data bus
70	P1.11	I/O	D	GPIO1 pin 11
	CIS_D5	I	2	CMOS image sensor output data
	LCD_D5/ 8080_D5	O	4	TFT-LCD data bus/ 8080 CPU data bus
71	P1.10	I/O	D	GPIO1 pin 10
	CIS_D4	I	2	CMOS image sensor output data
	LCD_D4/ 8080_D4	O	4	TFT-LCD data bus/ 8080 CPU data bus
72	P0.10	I/O	D	GPIO0 pin 10
	SPIFC_MISO	I	1	SPI NOR flash master in slave out
	SPI0DMA_MISO	I	3	SPI0 with DMA master in slave out
73	P0.0	I/O	D	GPIO0 pin 0
	I2C0_SCL	O	1	I²C0 serial clock
74	VSS	GND	–	Ground
75	P0.1	I/O	D	GPIO0 pin 1
	I2C0_SDA	I/O	1	I²C0 serial data
76	P3.14	I/O	D	GPIO3 pin 14
	SPI1_MISO	I/O[3]	1	SPI1 master in slave out
	SPI1DMA_MISO	I	4	SPI1 with DMA master in slave out
	CT32B2_CAP0	I	6	32-bit timer/counter 2 capture channel 0
	CT32B3_PWM0	O	7	32-bit timer/counter 3 pulse width modulation data output 0
77	P3.15	I/O	D	GPIO3 pin 15
	SPI1_MOSI	I/O[4]	1	SPI1 master out slave in
	SPI1DMA_MOSI	O	4	SPI1 with DMA master out slave in
	CT32B3_CAP0	I	6	32-bit timer/counter 3 capture channel 0
	CT32B2_PWM2	O	7	32-bit timer/counter 2 pulse width modulation data output 2
78	P3.12	I/O	D	GPIO3 pin 12
	SPI1_CS	I/O[4]	1	SPI1 chip select
	SPI1DMA_CS	O	4	SPI1 with DMA chip select
	CT32B0_CAP0	I	6	32-bit timer/counter 0 capture channel 0
	CT32B3_PWM2	O	7	32-bit timer/counter 3 pulse width modulation data output 2

[3] Operates as input in master mode, output in slave mode.
[4] Operates as output in master mode, input in slave mode.

No.	Name	Type[1]	Mode[2]	Description
79	P3.13	I/O	D	GPIO3 pin 13
	SPI1_SCLK	I/O[4]	1	SPI1 serial clock
	SPI1DMA_SCLK	O	4	SPI1 with DMA serial clock
	CT32B1_CAP0	I	6	32-bit timer/counter 1 capture channel 0
	CT32B3_PWM1	O	7	32-bit timer/counter 3 pulse width modulation data output 1
80	VDD33	P	–	3.3V power supply

3.1.3 Pinmux

Table 3–2 Pinmux Overview for SNC73520[5]

Default	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
P0.0	I2C0_SCL	–	–	–	–	–	–
P0.1	I2C0_SDA	–	–	–	–	–	–
P0.2	UART0_TXD	–	–	–	–	–	CT32B7_PWM2
P0.3	UART0_RXD	–	–	–	–	–	CT32B7_PWM1
P0.4	AIN0	–	–	–	–	–	CT32B7_PWM0
P0.5	AIN1	–	–	–	–	–	CT32B6_PWM2
P0.6	AIN2	–	–	–	–	–	CT32B6_PWM1
P0.7	AIN3	–	–	–	–	–	CT32B6_PWM0
P0.8	SPIFC_CS	–	SPI0DMA_CS	–	–	–	–
P0.9	SPIFC_CLK	–	SPI0DMA_SCLK	–	–	–	–
P0.10	SPIFC_MISO	–	SPI0DMA_MISO	–	–	–	–
P0.11	SPIFC_MOSI	–	SPI0DMA_MOSI	–	–	–	–
P0.13	–	–	–	–	–	–	CT32B0_PWM0
P1.2	–	CIS_VSYNC	–	LCD_HSYNC/ 8080_RD	–	–	–
P1.3	–	CIS_HSYNC	–	LCD_VSYNC/ 8080_WR	–	–	–
P1.4	SD0_CLK	CIS_MCLK	–	LCD_DE/ 8080_CS	SPI0DMA_CS	–	CT32B7_PWM2
P1.5	SD0_CMD	CIS_PCLK	–	LCD_DCLK/ 8080_A0	SPI0DMA_SCLK	–	CT32B7_PWM1
P1.6	SD0_D0	CIS_D0	–	LCD_D0/ 8080_D0	SPI0DMA_MISO	–	CT32B7_PWM0
P1.7	SD0_D1	CIS_D1	–	LCD_D1/ 8080_D1	SPI0DMA_MOSI	–	CT32B6_PWM2
P1.8	SD0_D2	CIS_D2	–	LCD_D2/ 8080_D2	SPI0DMA_MISO2	–	CT32B6_PWM1
P1.9	SD0_D3	CIS_D3	–	LCD_D3/ 8080_D3	SPI0DMA_MISO3	–	CT32B6_PWM0
P1.10	–	CIS_D4	–	LCD_D4/ 8080_D4	–	–	–
P1.11	–	CIS_D5	–	LCD_D5/ 8080_D5	–	–	–
P1.12	–	CIS_D6	–	LCD_D6/ 8080_D6	–	–	–

[5] "–" represents reserved pinmux options.

Default	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
P1.13	–	CIS_D7	–	LCD_D7/ 8080_D7	–	–	–
P1.14	SDIO_CLK	–	–	–	I2S4_MCLK	–	–
P1.15	SDIO_CMD	–	–	–	I2S4_DIN	–	–
P2.0	SDIO_D0	–	–	–	I2S4_DOUT	–	–
P2.1	SDIO_D1	–	–	–	I2S4_BCLK	–	–
P2.2	SDIO_D2	–	–	–	I2S4_WS	–	–
P2.3	SDIO_D3	–	–	–	–	–	–
P2.4	LCD_HSYNC	8080_RD	–	–	I2S4_MCLK	–	CT32B5_PWM2
P2.5	LCD_VSYNC	8080_WR	–	–	I2S4_DIN	–	CT32B5_PWM1
P2.6	LCD_DE	8080_CS	–	–	I2S4_DOUT	–	CT32B5_PWM0
P2.7	LCD_DCLK	8080_A0	–	–	I2S4_BCLK	–	CT32B4_PWM2
P2.8	LCD_D0	8080_D0	–	–	I2S4_WS	–	–
P2.9	LCD_D1	8080_D1	–	–	–	–	–
P2.10	LCD_D2	8080_D2	–	–	–	–	–
P2.11	LCD_D3	8080_D3	–	–	–	–	–
P2.12	LCD_D4	8080_D4	–	–	–	–	–
P2.13	LCD_D5	8080_D5	–	–	–	–	–
P2.14	LCD_D6	8080_D6	–	–	–	–	–
P2.15	LCD_D7	8080_D7	–	–	–	–	–
P3.4	–	–	–	–	–	I2S1_DIN	–
P3.5	–	–	–	–	–	I2S1_BCLK	–
P3.6	–	–	–	–	–	I2S1_WS	–
P3.12	SPI1_CS	–	–	SPI1DMA_CS	–	CT32B0_CAP0	CT32B3_PWM2
P3.13	SPI1_SCLK	–	–	SPI1DMA_SCLK	–	CT32B1_CAP0	CT32B3_PWM1
P3.14	SPI1_MISO	–	–	SPI1DMA_MISO	–	CT32B2_CAP0	CT32B3_PWM0
P3.15	SPI1_MOSI	–	–	SPI1DMA_MOSI	–	CT32B3_CAP0	CT32B2_PWM2
SWO	P4.5	–	–	–	–	–	CT32B0_PWM2
SWCLK	P4.6	–	–	–	–	–	CT32B0_PWM1
SWDIO	P4.7	–	–	–	–	–	CT32B0_PWM0
P4.8	I2C1_SCL	–	–	–	–	–	CT32B3_PWM2
P4.9	I2C1_SDA	–	–	–	–	–	CT32B3_PWM1
P4.10	I2S0_ DIN	–	–	–	–	–	CT32B3_PWM0
P4.11	I2S0_BCLK	–	–	–	–	–	CT32B2_PWM2
P4.12	I2S0_WS		–	–	–	–	–

3.2 SNC73521

3.2.1 Pin Diagram

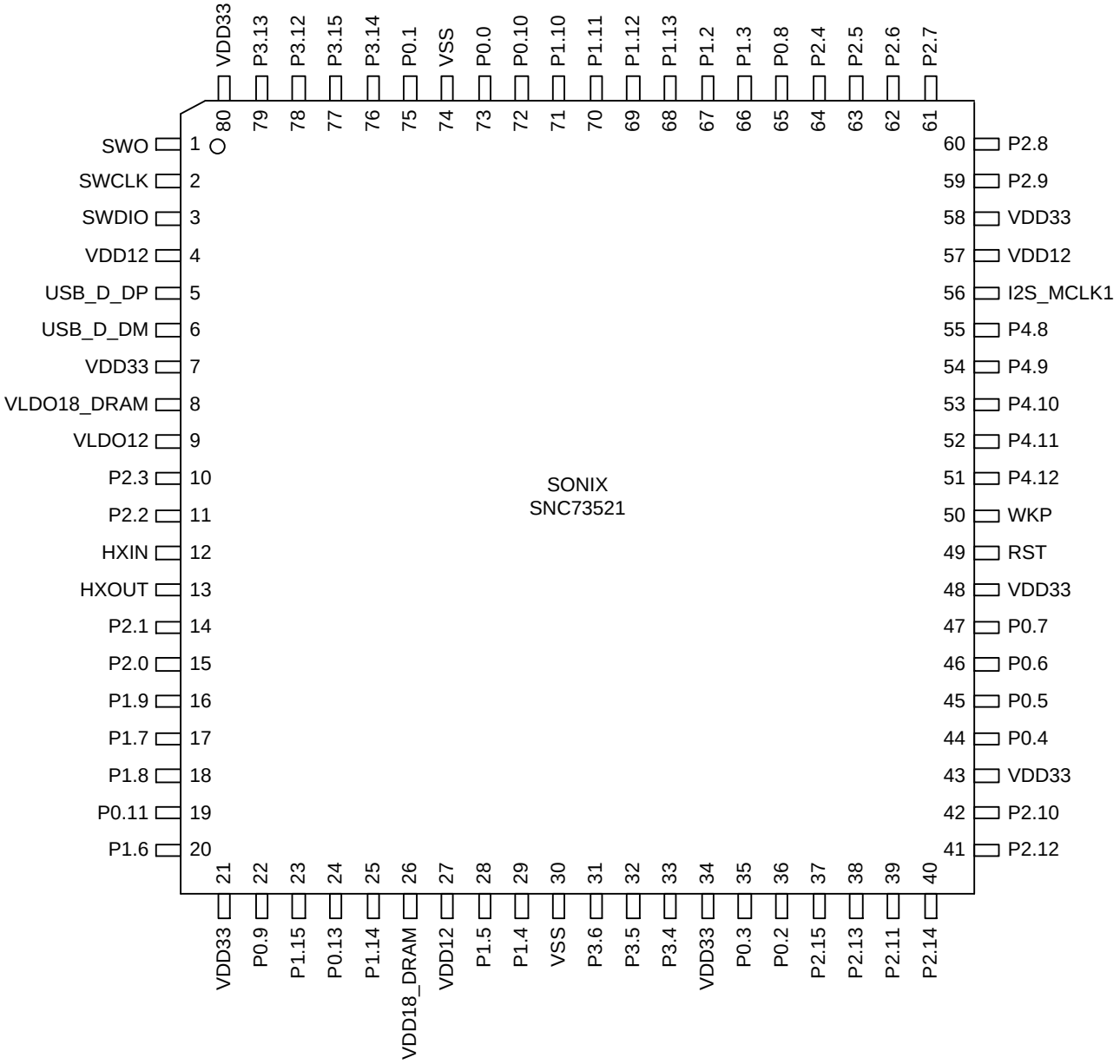


Figure 3–2 SNC73521 Pin Diagram

3.2.2 Pin Description

Table 3–3 SNC73521 Pin Description

No.	Name	Type[6]	Mode[7]	Description
1	SWO	O	D	Serial wire output trace port
	P4.5	I/O	1	GPIO4 pin 5
	CT32B0_PWM2	O	7	32-bit timer/counter 0 pulse width modulation data output 2
2	SWCLK	O	D	Serial wire clock
	P4.6	I/O	1	GPIO4 pin 6
	CT32B0_PWM1	O	7	32-bit timer/counter 0 pulse width modulation data output 1
3	SWDIO	I/O	D	Serial wire debug bi-directional data. A pull-up resistor, 100 kΩ recommended by ARM, is required.
	P4.7	I/O	1	GPIO4 pin 7
	CT32B0_PWM0	O	7	32-bit timer/counter 0 pulse width modulation data output 0
4	VDD12	P	–	1.2V power supply
5	USB_D_DP	A I/O	–	USB D+ signal
6	USB_D_DM	A I/O	–	USB D- signal
7	VDD33	P	–	3.3V power supply
8	VLDO18_DRAM	P	–	1.8V power for DRAM; powered from low dropout regulator (LDO)
9	VLDO12	P	–	Internal 1.2V LDO output
10	P2.3	I/O	D	GPIO2 pin 3
	SDIO_D3	I/O	1	SD/SDIO (SD1) data
11	P2.2	I/O	D	GPIO2 pin 2
	SDIO_D2	I/O	1	SD/SDIO (SD1) data
	I2S4_WS	I/O	5	I²S4 word select
12	HXIN	I	–	External 12 MHz crystal input
13	HXOUT	O	–	External 12 MHz crystal output
14	P2.1	I/O	D	GPIO2 pin 1
	SDIO_D1	I/O	1	SD/SDIO (SD1) data
	I2S4_BCLK	I/O	5	I²S4 bit clock. Bit clock can be programmed as a master or a slave.
15	P2.0	I/O	D	GPIO2 pin 0
	SDIO_D0	I/O	1	SD/SDIO (SD1) data
	I2S4_DOUT	O	5	I²S4 data output
16	P1.9	I/O	D	GPIO1 pin 9
	SD0_D3	I/O	1	SD0 data
	CIS_D3	I	2	CMOS image sensor output data
	LCD_D3/ 8080_D3	O	4	TFT-LCD data bus/ 8080 CPU data bus
	SPI0DMA_MISO3	I	5	SPI0 with DMA master in slave out
	CT32B6_PWM0	O	7	32-bit timer/counter 6 pulse width modulation data output 0
17	P1.7	I/O	D	GPIO1 pin 7
	SD0_D1	I/O	1	SD0 data
	CIS_D1	I	2	CMOS image sensor output data
	LCD_D1/ 8080_D1	O	4	TFT-LCD data bus/ 8080 CPU data bus
	SPI0DMA_MOSI	O	5	SPI0 with DMA master out slave in
	CT32B6_PWM2	O	7	32-bit timer/counter 6 pulse width modulation data output 2
18	P1.8	I/O	D	GPIO1 pin 8
	SD0_D2	I/O	1	SD0 data
	CIS_D2	I	2	CMOS image sensor output data
	LCD_D2/ 8080_D2	O	4	TFT-LCD data bus/ 8080 CPU data bus
	SPI0DMA_MISO2	I	5	SPI0 with DMA master in slave out
	CT32B6_PWM1	O	7	32-bit timer/counter 6 pulse width modulation data output 1

[6] Signal Types:
I = Input
O = Output
A = Analog signal
P = Power
GND = Ground

[7] D = Default

No.	Name	Type[6]	Mode[7]	Description
19	P0.11	I/O	D	GPIO0 pin 11
	SPIFC_MOSI	O	1	SPI NOR flash master out slave in
	SPI0DMA_MOSI	O	3	SPI0 with DMA master out slave in
20	P1.6	I/O	D	GPIO1 pin 6
	SD0_D0	I/O	1	SD0 data
	CIS_D0	I	2	CMOS image sensor output data
	LCD_D0/ 8080_D0	O	4	TFT-LCD data bus/ 8080 CPU data bus
	SPI0DMA_MISO	I	5	SPI0 with DMA master in slave out
	CT32B7_PWM0	O	7	32-bit timer/counter 7 pulse width modulation data output 0
21	VDD33	P	–	3.3V power supply
22	P0.9	I/O	D	GPIO0 pin 9
	SPIFC_CLK	O	1	SPI NOR flash clock output
	SPI0DMA_SCLK	O	3	SPI0 with DMA serial clock
23	P1.15	I/O	D	GPIO1 pin 15
	SDIO_CMD	O	1	SD/SDIO (SD1) command
	I2S4_DIN	I	5	I²S4 data input
24	P0.13	I/O	D	GPIO0 pin 13
	CT32B0_PWM0	O	7	32-bit timer/counter 0 pulse width modulation data output 0
25	P1.14	I/O	D	GPIO1 pin 14
	SDIO_CLK	O	1	SD/SDIO (SD1) clock output
	I2S4_MCLK	I/O	5	I²S4 master clock
26	VDD18_DRAM	P	–	1.8V power supply for DRAM
27	VDD12	P	–	1.2V power supply
28	P1.5	I/O	D	GPIO1 pin 5
	SD0_CMD	O	1	SD0 command
	CIS_PCLK	I	2	CMOS image sensor pixel clock
	LCD_DCLK/ 8080_A0	O	4	TFT-LCD clock/ 8080 CPU address 0
	SPI0DMA_SCLK	O	5	SPI0 with DMA serial clock
	CT32B7_PWM1	O	7	32-bit timer/counter 7 pulse width modulation data output 1
29	P1.4	I/O	D	GPIO1 pin 4
	SD0_CLK	O	1	SD0 clock output
	CIS_MCLK	O	2	CMOS image sensor master clock
	LCD_DE/ 8080_CS	O	4	TFT-LCD data enable/ 8080 CPU chip select; active low
	SPI0DMA_CS	O	5	SPI0 with DMA chip select
	CT32B7_PWM2	O	7	32-bit timer/counter 7 pulse width modulation data output 2
30	VSS	GND	–	Ground
31	P3.6	I/O	D	GPIO3 pin 6
	I2S1_WS	I/O	6	I²S1 word select
32	P3.5	I/O	D	GPIO3 pin 5
	I2S1_BCLK	I/O	6	I²S1 bit clock. Bit clock can be programmed as a master or a slave.
33	P3.4	I/O	D	GPIO3 pin 4
	I2S1_DIN	I	6	I²S1 data input
34	VDD33	P	–	3.3V power supply
35	P0.3	I/O	D	GPIO0 pin 3
	UART0_RXD	I	1	UART0 serial receive data
	CT32B7_PWM1	O	7	32-bit timer/counter 7 pulse width modulation data output 1
36	P0.2	I/O	D	GPIO0 pin 2
	UART0_TXD	O	1	UART0 serial transmit data
	CT32B7_PWM2	O	7	32-bit timer/counter 7 pulse width modulation data output 2
37	P2.15	I/O	D	GPIO2 pin 15
	LCD_D7	O	1	TFT-LCD data bus
	8080_D7	O	2	8080 CPU data bus
38	P2.13	I/O	D	GPIO2 pin 13
	LCD_D5	O	1	TFT-LCD data bus
	8080_D5	O	2	8080 CPU data bus
39	P2.11	I/O	D	GPIO2 pin 11
	LCD_D3	O	1	TFT-LCD data bus
	8080_D3	O	2	8080 CPU data bus

No.	Name	Type[6]	Mode[7]	Description
40	P2.14	I/O	D	GPIO2 pin 14
	LCD_D6	O	1	TFT-LCD data bus
	8080_D6	O	2	8080 CPU data bus
41	P2.12	I/O	D	GPIO2 pin 12
	LCD_D4	O	1	TFT-LCD data bus
	8080_D4	O	2	8080 CPU data bus
42	P2.10	I/O	D	GPIO2 pin 10
	LCD_D2	O	1	TFT-LCD data bus
	8080_D2	O	2	8080 CPU data bus
43	VDD33	P	–	3.3V power supply
44	P0.4	I/O	D	GPIO0 pin 4
	AIN0	I	1	ADC input channel 0
	CT32B7_PWM0	O	7	32-bit timer/counter 7 pulse width modulation data output 0
45	P0.5	I/O	D	GPIO0 pin 5
	AIN1	I	1	ADC input channel 1
	CT32B6_PWM2	O	7	32-bit timer/counter 6 pulse width modulation data output 2
46	P0.6	I/O	D	GPIO0 pin 6
	AIN2	I	1	ADC input channel 2
	CT32B6_PWM1	O	7	32-bit timer/counter 6 pulse width modulation data output 1
47	P0.7	I/O	D	GPIO0 pin 7
	AIN3	I	1	ADC input channel 3
	CT32B6_PWM0	O	7	32-bit timer/counter 6 pulse width modulation data output 0
48	VDD33	P	–	3.3V power supply
49	RST	I	–	Reset pin
50	WKP	I	–	Wakeup pin
51	P4.12	I/O	D	GPIO4 pin 12
	I2S0_WS	I/O	1	I²S0 word select
52	P4.11	I/O	D	GPIO4 pin 11
	I2S0_BCLK	I/O	1	I²S0 bit clock. Bit clock can be programmed as a master or a slave.
	CT32B2_PWM2	O	7	32-bit timer/counter 2 pulse width modulation data output 2
53	P4.10	I/O	D	GPIO4 pin 10
	I2S0_DIN	I	1	I²S0 data input
	CT32B3_PWM0	O	7	32-bit timer/counter 3 pulse width modulation data output 0
54	P4.9	I/O	D	GPIO4 pin 9
	I2C1_SDA	I/O	1	I²C1 serial data
	CT32B3_PWM1	O	7	32-bit timer/counter 3 pulse width modulation data output 1
55	P4.8	I/O	D	GPIO4 pin 8
	I2C1_SCL	O	1	I²C1 serial clock
	CT32B3_PWM2	O	7	32-bit timer/counter 3 pulse width modulation data output 2
56	I2S_MCLK1	O	–	I²S master clock output 1
57	VDD12	P	–	1.2V power supply
58	VDD33	P	–	3.3V power supply
59	P2.9	I/O	D	GPIO2 pin 9
	LCD_D1	O	1	TFT-LCD data bus
	8080_D1	O	2	8080 CPU data bus
60	P2.8	I/O	D	GPIO2 pin 8
	LCD_D0	O	1	TFT-LCD data bus
	8080_D0	O	2	8080 CPU data bus
	I2S4_WS	I/O	5	I²S4 word select
61	P2.7	I/O	D	GPIO2 pin 7
	LCD_DCLK	O	1	TFT-LCD clock
	8080_A0	O	2	8080 CPU address 0
	I2S4_BCLK	I/O	5	I²S4 bit clock. Bit clock can be programmed as a master or a slave.
	CT32B4_PWM2	O	7	32-bit timer/counter 4 pulse width modulation data output 2
62	P2.6	I/O	D	GPIO2 pin 6
	LCD_DE	O	1	TFT-LCD data enable
	8080_CS	O	2	8080 CPU chip select; active low
	I2S4_DOUT	O	5	I²S4 data output
	CT32B5_PWM0	O	7	32-bit timer/counter 5 pulse width modulation data output 0

No.	Name	Type[6]	Mode[7]	Description
63	P2.5	I/O	D	GPIO2 pin 5
	LCD_VSYNC	O	1	TFT-LCD vertical/frame synchronization
	8080_WR	O	2	8080 CPU write; active low
	I2S4_DIN	I	5	I²S4 data input
	CT32B5_PWM1	O	7	32-bit timer/counter 5 pulse width modulation data output 1
64	P2.4	I/O	D	GPIO2 pin 4
	LCD_HSYNC	O	1	TFT-LCD horizontal/line synchronization
	8080_RD	O	2	8080 CPU read; active low
	I2S4_MCLK	I/O	5	I²S4 master clock
	CT32B5_PWM2	O	7	32-bit timer/counter 5 pulse width modulation data output 2
65	P0.8	I/O	D	GPIO0 pin 8
	SPIFC_CS	O	1	SPI NOR flash chip select
	SPI0DMA_CS	O	3	SPI0 with DMA chip select
66	P1.3	I/O	D	GPIO1 pin 3
	CIS_HSYNC	I	2	CMOS image sensor output horizontal sync
	LCD_VSYNC/ 8080_WR	O	4	TFT-LCD vertical/frame synchronization/ 8080 CPU write; active low
67	P1.2	I/O	D	GPIO1 pin 2
	CIS_VSYNC	I	2	CMOS image sensor output vertical sync
	LCD_HSYNC/ 8080_RD	O	4	TFT-LCD horizontal/line synchronization/ 8080 CPU read; active low
68	P1.13	I/O	D	GPIO1 pin 13
	CIS_D7	I	2	CMOS image sensor output data
	LCD_D7/ 8080_D7	O	4	TFT-LCD data bus/ 8080 CPU data bus
69	P1.12	I/O	D	GPIO1 pin 12
	CIS_D6	I	2	CMOS image sensor output data
	LCD_D6/ 8080_D6	O	4	TFT-LCD data bus/ 8080 CPU data bus
70	P1.11	I/O	D	GPIO1 pin 11
	CIS_D5	I	2	CMOS image sensor output data
	LCD_D5/ 8080_D5	O	4	TFT-LCD data bus/ 8080 CPU data bus
71	P1.10	I/O	D	GPIO1 pin 10
	CIS_D4	I	2	CMOS image sensor output data
	LCD_D4/ 8080_D4	O	4	TFT-LCD data bus/ 8080 CPU data bus
72	P0.10	I/O	D	GPIO0 pin 10
	SPIFC_MISO	I	1	SPI NOR flash master in slave out
	SPI0DMA_MISO	I	3	SPI0 with DMA master in slave out
73	P0.0	I/O	D	GPIO0 pin 0
	I2C0_SCL	O	1	I²C0 serial clock
74	VSS	GND	–	Ground
75	P0.1	I/O	D	GPIO0 pin 1
	I2C0_SDA	I/O	1	I²C0 serial data
76	P3.14	I/O	D	GPIO3 pin 14
	SPI1_MISO	I/O[8]	1	SPI1 master in slave out
	SPI1DMA_MISO	I	4	SPI1 with DMA master in slave out
	CT32B2_CAP0	I	6	32-bit timer/counter 2 capture channel 0
	CT32B3_PWM0	O	7	32-bit timer/counter 3 pulse width modulation data output 0
77	P3.15	I/O	D	GPIO3 pin 15
	SPI1_MOSI	I/O[9]	1	SPI1 master out slave in
	SPI1DMA_MOSI	O	4	SPI1 with DMA master out slave in
	CT32B3_CAP0	I	6	32-bit timer/counter 3 capture channel 0
	CT32B2_PWM2	O	7	32-bit timer/counter 2 pulse width modulation data output 2

[8] Operates as input in master mode, output in slave mode.
[9] Operates as output in master mode, input in slave mode.

No.	Name	Type[6]	Mode[7]	Description
78	P3.12	I/O	D	GPIO3 pin 12
	SPI1_CS	I/O[9]	1	SPI1 chip select
	SPI1DMA_CS	O	4	SPI1 with DMA chip select
	CT32B0_CAP0	I	6	32-bit timer/counter 0 capture channel 0
	CT32B3_PWM2	O	7	32-bit timer/counter 3 pulse width modulation data output 2
79	P3.13	I/O	D	GPIO3 pin 13
	SPI1_SCLK	I/O[9]	1	SPI1 serial clock
	SPI1DMA_SCLK	O	4	SPI1 with DMA serial clock
	CT32B1_CAP0	I	6	32-bit timer/counter 1 capture channel 0
	CT32B3_PWM1	O	7	32-bit timer/counter 3 pulse width modulation data output 1
80	VDD33	P	–	3.3V power supply

3.2.3 Pinmux

Table 3–4 Pinmux Overview for SNC73521[10]

Default	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
P0.0	I2C0_SCL	–	–	–	–	–	–
P0.1	I2C0_SDA	–	–	–	–	–	–
P0.2	UART0_TXD	–	–	–	–	–	CT32B7_PWM2
P0.3	UART0_RXD	–	–	–	–	–	CT32B7_PWM1
P0.4	AIN0	–	–	–	–	–	CT32B7_PWM0
P0.5	AIN1	–	–	–	–	–	CT32B6_PWM2
P0.6	AIN2	–	–	–	–	–	CT32B6_PWM1
P0.7	AIN3	–	–	–	–	–	CT32B6_PWM0
P0.8	SPIFC_CS	–	SPI0DMA_CS	–	–	–	–
P0.9	SPIFC_CLK	–	SPI0DMA_SCLK	–	–	–	–
P0.10	SPIFC_MISO	–	SPI0DMA_MISO	–	–	–	–
P0.11	SPIFC_MOSI	–	SPI0DMA_MOSI	–	–	–	–
P0.13	–	–	–	–	–	–	CT32B0_PWM0
P1.2	–	CIS_VSYNC	–	LCD_HSYNC/ 8080_RD	–	–	–
P1.3	–	CIS_HSYNC	–	LCD_VSYNC/ 8080_WR	–	–	–
P1.4	SD0_CLK	CIS_MCLK	–	LCD_DE/ 8080_CS	SPI0DMA_CS	–	CT32B7_PWM2
P1.5	SD0_CMD	CIS_PCLK	–	LCD_DCLK/ 8080_A0	SPI0DMA_SCLK	–	CT32B7_PWM1
P1.6	SD0_D0	CIS_D0	–	LCD_D0/ 8080_D0	SPI0DMA_MISO	–	CT32B7_PWM0
P1.7	SD0_D1	CIS_D1	–	LCD_D1/ 8080_D1	SPI0DMA_MOSI	–	CT32B6_PWM2
P1.8	SD0_D2	CIS_D2	–	LCD_D2/ 8080_D2	SPI0DMA_MISO2	–	CT32B6_PWM1
P1.9	SD0_D3	CIS_D3	–	LCD_D3/ 8080_D3	SPI0DMA_MISO3	–	CT32B6_PWM0
P1.10	–	CIS_D4	–	LCD_D4/ 8080_D4	–	–	–
P1.11	–	CIS_D5	–	LCD_D5/ 8080_D5	–	–	–
P1.12	–	CIS_D6	–	LCD_D6/ 8080_D6	–	–	–

[10] "–" represents reserved pinmux options.

Default	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
P1.13	–	CIS_D7	–	LCD_D7/ 8080_D7	–	–	–
P1.14	SDIO_CLK	–	–	–	I2S4_MCLK	–	–
P1.15	SDIO_CMD	–	–	–	I2S4_DIN	–	–
P2.0	SDIO_D0	–	–	–	I2S4_DOUT	–	–
P2.1	SDIO_D1	–	–	–	I2S4_BCLK	–	–
P2.2	SDIO_D2	–	–	–	I2S4_WS	–	–
P2.3	SDIO_D3	–	–	–	–	–	–
P2.4	LCD_HSYNC	8080_RD	–	–	I2S4_MCLK	–	CT32B5_PWM2
P2.5	LCD_VSYNC	8080_WR	–	–	I2S4_DIN	–	CT32B5_PWM1
P2.6	LCD_DE	8080_CS	–	–	I2S4_DOUT	–	CT32B5_PWM0
P2.7	LCD_DCLK	8080_A0	–	–	I2S4_BCLK	–	CT32B4_PWM2
P2.8	LCD_D0	8080_D0	–	–	I2S4_WS	–	–
P2.9	LCD_D1	8080_D1	–	–	–	–	–
P2.10	LCD_D2	8080_D2	–	–	–	–	–
P2.11	LCD_D3	8080_D3	–	–	–	–	–
P2.12	LCD_D4	8080_D4	–	–	–	–	–
P2.13	LCD_D5	8080_D5	–	–	–	–	–
P2.14	LCD_D6	8080_D6	–	–	–	–	–
P2.15	LCD_D7	8080_D7	–	–	–	–	–
P3.4	–	–	–	–	–	I2S1_DIN	–
P3.5	–	–	–	–	–	I2S1_BCLK	–
P3.6	–	–	–	–	–	I2S1_WS	–
P3.12	SPI1_CS	–	–	SPI1DMA_CS	–	CT32B0_CAP0	CT32B3_PWM2
P3.13	SPI1_SCLK	–	–	SPI1DMA_SCLK	–	CT32B1_CAP0	CT32B3_PWM1
P3.14	SPI1_MISO	–	–	SPI1DMA_MISO	–	CT32B2_CAP0	CT32B3_PWM0
P3.15	SPI1_MOSI	–	–	SPI1DMA_MOSI	–	CT32B3_CAP0	CT32B2_PWM2
SWO	P4.5	–	–	–	–	–	CT32B0_PWM2
SWCLK	P4.6	–	–	–	–	–	CT32B0_PWM1
SWDIO	P4.7	–	–	–	–	–	CT32B0_PWM0
P4.8	I2C1_SCL	–	–	–	–	–	CT32B3_PWM2
P4.9	I2C1_SDA	–	–	–	–	–	CT32B3_PWM1
P4.10	I2S0_ DIN	–	–	–	–	–	CT32B3_PWM0
P4.11	I2S0_BCLK	–	–	–	–	–	CT32B2_PWM2
P4.12	I2S0_WS		–	–	–	–	–

3.3 SNC73522

3.3.1 Pin Diagram

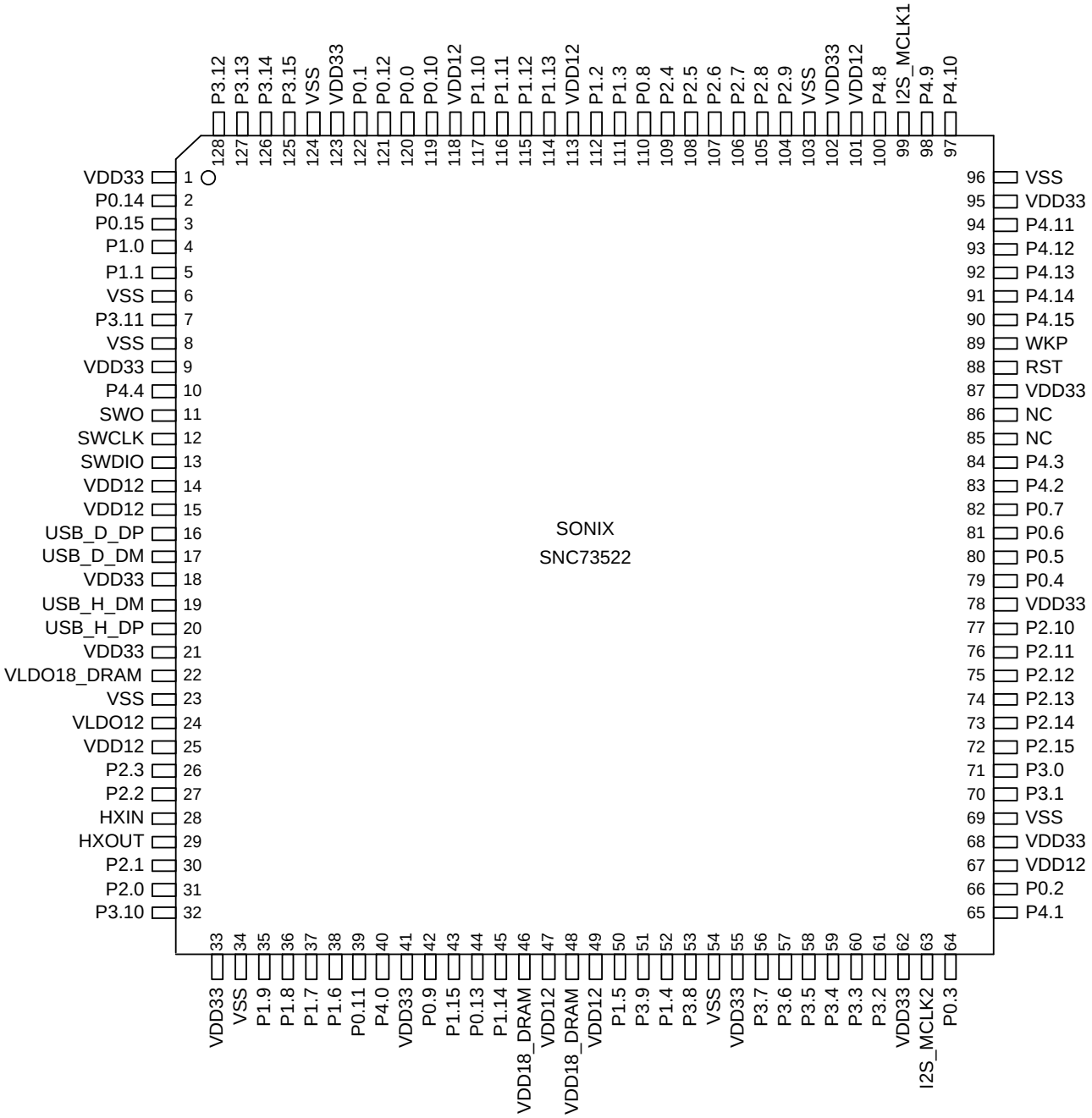


Figure 3–3 SNC73522 Pin Diagram

3.3.2 Pin Description

Table 3–5 SNC73522 Pin Description

No.	Name	Type[11]	Mode[12]	Description
1	VDD33	P	–	3.3V power supply
2	P0.14	I/O	D	GPIO0 pin 14
	CLKOUT	O	2	Clock output
	SPI0_CS	I/O[13]	4	SPI0 chip select
3	P0.15	I/O	D	GPIO0 pin 15
	NAND_CE	O	3	NAND flash chip enable
	SPI0_SCLK	I/O[13]	4	SPI0 serial clock
4	P1.0	I/O	D	GPIO1 pin 0
	NAND_RB	O	3	NAND flash ready/busy output
	SPI0_MISO	I/O[14]	4	SPI0 master in slave out
5	P1.1	I/O	D	GPIO1 pin 1
	NAND_ALE	O	3	NAND flash address latch enable
	SPI0_MOSI	I/O[13]	4	SPI0 master out slave in
6	VSS	GND	–	Ground
7	P3.11	I/O	D	GPIO3 pin 11
	NAND_D4	I/O	3	NAND flash data input/output
	CT32B4_PWM0	O	7	32-bit timer/counter 4 pulse width modulation data output 0
8	VSS	GND	–	Ground
9	VDD33	P	–	3.3V power supply
10	P4.4	I/O	D	GPIO4 pin4
	CT32B1_PWM0	O	7	32-bit timer/counter 1 pulse width modulation data output 0
11	SWO	O	D	Serial wire output trace port
	P4.5	I/O	1	GPIO4 pin 5
	CT32B0_PWM2	O	7	32-bit timer/counter 0 pulse width modulation data output 2
12	SWCLK	O	D	Serial wire clock
	P4.6	I/O	1	GPIO4 pin 6
	CT32B0_PWM1	O	7	32-bit timer/counter 0 pulse width modulation data output 1
13	SWDIO	I/O	D	Serial wire debug bi-directional data. A pull-up resistor, 100 kΩ recommended by ARM, is required.
	P4.7	I/O	1	GPIO4 pin 7
	CT32B0_PWM0	O	7	32-bit timer/counter 0 pulse width modulation data output 0
14	VDD12	P	–	1.2V power supply
15	VDD12	P	–	1.2V power supply
16	USB_D_DP	A I/O	–	USB D+ signal
17	USB_D_DM	A I/O	–	USB D- signal
18	VDD33	P	–	3.3V power supply
19	USB_H_DM	A I/O	–	USB H- signal
20	USB_H_DP	A I/O	–	USB H+ signal
21	VDD33	P	–	3.3V power supply
22	VLDO18_DRAM	P	–	1.8V power for DRAM; powered from low dropout regulator (LDO)
23	VSS	GND	–	Ground
24	VLDO12	P	–	Internal 1.2V LDO output
25	VDD12	P	–	1.2V power supply
26	P2.3	I/O	D	GPIO2 pin 3
	SDIO_D3	I/O	1	SD/SDIO (SD1) data
27	P2.2	I/O	D	GPIO2 pin 2
	SDIO_D2	I/O	1	SD/SDIO (SD1) data
	I2S4_WS	I/O	5	I^2S4 word select
28	HXIN	I	–	External 12 MHz crystal input

[11] Signal Types:
I = Input
O = Output
A = Analog signal
P = Power
GND = Ground

[12] D = Default

[13] Operates as output in master mode, input in slave mode.

[14] Operates as input in master mode, output in slave mode.

No.	Name	Type[11]	Mode[12]	Description
29	HXOUT	O	–	External 12 MHz crystal output
30	P2.1	I/O	D	GPIO2 pin 1
	SDIO_D1	I/O	1	SD/SDIO (SD1) data
	I2S4_BCLK	I/O	5	I²S4 bit clock. Bit clock can be programmed as a master or a slave.
31	P2.0	I/O	D	GPIO2 pin 0
	SDIO_D0	I/O	1	SD/SDIO (SD1) data
	I2S4_DOUT	O	5	I²S4 data output
32	P3.10	I/O	D	GPIO3 pin 10
	NAND_D3	I/O	3	NAND flash data input/output
	SD0_D3	I/O	4	SD0 data
	CT32B4_PWM1	O	7	32-bit timer/counter 4 pulse width modulation data output 1
33	VDD33	P	–	3.3V power supply
34	VSS	GND	–	Ground
35	P1.9	I/O	D	GPIO1 pin 9
	SD0_D3	I/O	1	SD0 data
	CIS_D3	I	2	CMOS image sensor output data
	NAND_D3	I/O	3	NAND flash data input/output
	LCD_D3/ 8080_D3	O	4	TFT-LCD data bus/ 8080 CPU data bus
	SPI0DMA_MISO3	I	5	SPI0 with DMA master in slave out
	CT32B6_PWM0	O	7	32-bit timer/counter 6 pulse width modulation data output 0
36	P1.8	I/O	D	GPIO1 pin 8
	SD0_D2	I/O	1	SD0 data
	CIS_D2	I	2	CMOS image sensor output data
	NAND_D2	I/O	3	NAND flash data input/output
	LCD_D2/ 8080_D2	O	4	TFT-LCD data bus/ 8080 CPU data bus
	SPI0DMA_MISO2	I	5	SPI0 with DMA master in slave out
	CT32B6_PWM1	O	7	32-bit timer/counter 6 pulse width modulation data output 1
37	P1.7	I/O	D	GPIO1 pin 7
	SD0_D1	I/O	1	SD0 data
	CIS_D1	I	2	CMOS image sensor output data
	NAND_D1	I/O	3	NAND flash data input/output
	LCD_D1/ 8080_D1	O	4	TFT-LCD data bus/ 8080 CPU data bus
	SPI0DMA_MOSI	O	5	SPI0 with DMA master out slave in
	CT32B6_PWM2	O	7	32-bit timer/counter 6 pulse width modulation data output 2
38	P1.6	I/O	D	GPIO1 pin 6
	SD0_D0	I/O	1	SD0 data
	CIS_D0	I	2	CMOS image sensor output data
	NAND_D0	I/O	3	NAND flash data input/output
	LCD_D0/ 8080_D0	O	4	TFT-LCD data bus/ 8080 CPU data bus
	SPI0DMA_MISO	I	5	SPI0 with DMA master in slave out
	CT32B7_PWM0	O	7	32-bit timer/counter 7 pulse width modulation data output 0
39	P0.11	I/O	D	GPIO0 pin 11
	SPIFC_MOSI	O	1	SPI NOR flash master out slave in
	SPI0DMA_MOSI	O	3	SPI0 with DMA master out slave in
40	P4.0	I/O	D	GPIO4 pin 0
	UART1_TXD	O	1	UART1 serial transmit data
	SPI1DMA_MISO2	I	4	SPI1 with DMA master in slave out
	CT32B4_CAP0	O	6	32-bit timer/counter 4 capture channel 0
	CT32B2_PWM1	O	7	32-bit timer/counter 2 pulse width modulation data output 1
41	VDD33	P	–	3.3V power supply
42	P0.9	I/O	D	GPIO0 pin 9
	SPIFC_CLK	O	1	SPI NOR flash clock output
	SPI0DMA_SCLK	O	3	SPI0 with DMA serial clock
43	P1.15	I/O	D	GPIO1 pin 15
	SDIO_CMD	O	1	SD/SDIO (SD1) command
	I2S4_DIN	I	5	I²S4 data input

No.	Name	Type[11]	Mode[12]	Description
44	P0.13	I/O	D	GPIO0 pin 13
	SPIFC_D3	I/O	1	SPI NOR flash 4 x I/O mode, data pin
	SPI0DMA_MISO3	I	3	SPI0 with DMA master in slave out
	CT32B0_PWM0	O	7	32-bit timer/counter 0 pulse width modulation data output 0
45	P1.14	I/O	D	GPIO1 pin 14
	SDIO_CLK	O	1	SD/SDIO (SD1) clock output
	I2S4_MCLK	I/O	5	I²S4 master clock
46	VDD18_DRAM	P	–	1.8V power supply for DRAM
47	VDD12	P	–	1.2V power supply
48	VDD18_DRAM	P	–	1.8V power supply for DRAM
49	VDD12	P	–	1.2V power supply
50	P1.5	I/O	D	GPIO1 pin 5
	SD0_CMD	O	1	SD0 command
	CIS_PCLK	I	2	CMOS image sensor pixel clock
	NAND_CLE	O	3	NAND flash command latch enable
	LCD_DCLK/ 8080_A0	O	4	TFT-LCD clock/ 8080 CPU address 0
	SPI0DMA_SCLK	O	5	SPI0 with DMA serial clock
	CT32B7_PWM1	O	7	32-bit timer/counter 7 pulse width modulation data output 1
51	P3.9	I/O	D	GPIO3 pin 9
	LCD_D17	O	1	TFT-LCD data bus
	NAND_D2	I/O	3	NAND flash data input/output
	SD0_D2	O	4	SD0 data
	I2S3_WS	I/O	6	I²S3 word select
52	P1.4	I/O	D	GPIO1 pin 4
	SD0_CLK	O	1	SD0 clock output
	CIS_MCLK	O	2	CMOS image sensor master clock
	NAND_WP	O	3	NAND flash write protect
	LCD_DE/ 8080_CS	O	4	TFT-LCD data enable/ 8080 CPU chip select; active low
	SPI0DMA_CS	O	5	SPI0 with DMA chip select
	CT32B7_PWM2	O	7	32-bit timer/counter 7 pulse width modulation data output 2
53	P3.8	I/O	D	GPIO3 pin 8
	LCD_D16	O	1	TFT-LCD data bus
	NAND_D1	I/O	3	NAND flash data input/output
	SD0_D1	O	4	SD0 data
	I2S3_BCLK	I/O	6	I²S3 bit clock. Bit clock can be programmed as a master or a slave.
54	VSS	GND	–	Ground
55	VDD33	P	–	3.3V power supply
56	P3.7	I/O	D	GPIO3 pin 7
	LCD_D15	O	1	TFT-LCD data bus
	8080_D15	O	2	8080 CPU data bus
	NAND_D0	I/O	3	NAND flash data input/output
	SD0_D0	I/O	4	SD0 data
	I2S3_DOUT	O	6	I²S3 data output
57	P3.6	I/O	D	GPIO3 pin 6
	LCD_D14	O	1	TFT-LCD data bus
	8080_D14	O	2	8080 CPU data bus
	NAND_CLE	O	3	NAND flash command latch enable
	SD0_CMD	O	4	SD0 command
	I2S4_WS	I/O	5	I²S4 word select
	I2S1_WS	I/O	6	I²S1 word select
58	P3.5	I/O	D	GPIO3 pin 5
	LCD_D13	O	1	TFT-LCD data bus
	8080_D13	O	2	8080 CPU data bus
	NAND_WP	O	3	NAND flash write protect
	SD0_CLK	O	4	SD0 clock output
	I2S4_BCLK	I/O	5	I²S4 bit clock. Bit clock can be programmed as a master or a slave.
	I2S1_BCLK	I/O	6	I²S1 bit clock. Bit clock can be programmed as a master or a slave.

No.	Name	Type[11]	Mode[12]	Description
59	P3.4	I/O	D	GPIO3 pin 4
	LCD_D12	O	1	TFT-LCD data bus
	8080_D12	O	2	8080 CPU data bus
	NAND_RE	O	3	NAND flash read enable
	I2S4_DOUT	O	5	I²S4 data output
	I2S1_DIN	I	6	I²S1 data input
60	P3.3	I/O	D	GPIO3 pin 3
	LCD_D11	O	1	TFT-LCD data bus
	8080_D11	O	2	8080 CPU data bus
	NAND_WE	O	3	NAND flash write enable
	I2S4_DIN	I	5	I²S4 data input
	I2C2_SDA	I/O	6	I²C2 serial data
61	P3.2	I/O	D	GPIO3 pin 2
	LCD_D10	O	1	TFT-LCD data bus
	8080_D10	O	2	8080 CPU data bus
	NAND_ALE	O	3	NAND flash address latch enable
	I2S4_MCLK	I/O	5	I²S4 master clock
	I2C2_SCL	O	6	I²C2 serial clock
62	VDD33	P	–	3.3V power supply
63	I2S_MCLK2	O	–	I²S master clock output 2
64	P0.3	I/O	D	GPIO0 pin 3
	UART0_RXD	I	1	UART0 serial receive data
	CT32B7_PWM1	O	7	32-bit timer/counter 7 pulse width modulation data output 1
65	P4.1	I/O	D	GPIO4 pin 1
	UART1_RXD	I	1	UART1 serial receive data
	SPI1DMA_MISO3	I	4	SPI1 with DMA master in slave out
	CT32B5_CAP0	I	6	32-bit timer/counter 5 capture channel 0
	CT32B2_PWM0	O	7	32-bit timer/counter 2 pulse width modulation data output 0
66	P0.2	I/O	D	GPIO0 pin 2
	UART0_TXD	O	1	UART0 serial transmit data
	CT32B7_PWM2	O	7	32-bit timer/counter 7 pulse width modulation data output 2
67	VDD12	P	–	1.2V power supply
68	VDD33	P	–	3.3V power supply
69	VSS	GND	–	Ground
70	P3.1	I/O	D	GPIO3 pin 1
	LCD_D9	O	1	TFT-LCD data bus
	8080_D9	O	2	8080 CPU data bus
	NAND_RB	O	3	NAND flash ready/busy output
71	P3.0	I/O	D	GPIO3 pin 0
	LCD_D8	O	1	TFT-LCD data bus
	8080_D8	O	2	8080 CPU data bus
	NAND_CE	O	3	NAND flash chip enable
72	P2.15	I/O	D	GPIO2 pin 15
	LCD_D7	O	1	TFT-LCD data bus
	8080_D7	O	2	8080 CPU data bus
73	P2.14	I/O	D	GPIO2 pin 14
	LCD_D6	O	1	TFT-LCD data bus
	8080_D6	O	2	8080 CPU data bus
74	P2.13	I/O	D	GPIO2 pin 13
	LCD_D5	O	1	TFT-LCD data bus
	8080_D5	O	2	8080 CPU data bus
75	P2.12	I/O	D	GPIO2 pin 12
	LCD_D4	O	1	TFT-LCD data bus
	8080_D4	O	2	8080 CPU data bus
76	P2.11	I/O	D	GPIO2 pin 11
	LCD_D3	O	1	TFT-LCD data bus
	8080_D3	O	2	8080 CPU data bus
77	P2.10	I/O	D	GPIO2 pin 10
	LCD_D2	O	1	TFT-LCD data bus
	8080_D2	O	2	8080 CPU data bus
78	VDD33	P	–	3.3V power supply

No.	Name	Type[11]	Mode[12]	Description
79	P0.4	I/O	D	GPIO0 pin 4
	AIN0	I	1	ADC input channel 0
	CT32B7_PWM0	O	7	32-bit timer/counter 7 pulse width modulation data output 0
80	P0.5	I/O	D	GPIO0 pin 5
	AIN1	I	1	ADC input channel 1
	CT32B6_PWM2	O	7	32-bit timer/counter 6 pulse width modulation data output 2
81	P0.6	I/O	D	GPIO0 pin 6
	AIN2	I	1	ADC input channel 2
	CT32B6_PWM1	O	7	32-bit timer/counter 6 pulse width modulation data output 1
82	P0.7	I/O	D	GPIO0 pin 7
	AIN3	I	1	ADC input channel 3
	CT32B6_PWM0	O	7	32-bit timer/counter 6 pulse width modulation data output 0
83	P4.2	I/O	D	GPIO4 pin 2
	AIN4	I	1	ADC input channel 4
	CT32B6_CAP0	I	6	32-bit timer/counter 6 capture channel 0
	CT32B1_PWM2	O	7	32-bit timer/counter 1 pulse width modulation data output 2
84	P4.3	I/O	D	GPIO4 pin 3
	AIN5	I	1	ADC input channel 5
	CT32B7_CAP0	I	6	32-bit timer/counter 7 capture channel 0
	CT32B1_PWM1	O	7	32-bit timer/counter 1 pulse width modulation data output 1
85	NC	–	–	Not connected
86	NC	–	–	Not connected
87	VDD33	P	–	3.3V power supply
88	RST	I	–	Reset pin
89	WKP	I	–	Wakeup pin
90	P4.15	I/O	D	GPIO4 pin 15
	I2S2_WS	I/O	1	I²S2 word select
	CIS_D7	I	2	CMOS image sensor output data
91	P4.14	I/O	D	GPIO4 pin 14
	I2S2_BCLK	I/O	1	I²S2 bit clock. Bit clock can be programmed as a master or a slave.
	CIS_D6	I	2	CMOS image sensor output data
92	P4.13	I/O	D	GPIO4 pin 13
	I2S2_DOUT	O	1	I²S2 data output
	CIS_D5	I	2	CMOS image sensor output data
93	P4.12	I/O	D	GPIO4 pin 12
	I2S0_WS	I/O	1	I²S0 word select
	CIS_D4	I	2	CMOS image sensor output data
94	P4.11	I/O	D	GPIO4 pin 11
	I2S0_BCLK	I/O	1	I²S0 bit clock. Bit clock can be programmed as a master or a slave.
	CT32B2_PWM2	O	7	32-bit timer/counter 2 pulse width modulation data output 2
95	VDD33	P	–	3.3V power supply
96	VSS	GND	–	Ground
97	P4.10	I/O	D	GPIO4 pin 10
	I2S0_DIN	I	1	I²S0 data input
	CT32B3_PWM0	O	7	32-bit timer/counter 3 pulse width modulation data output 0
98	P4.9	I/O	D	GPIO4 pin 9
	I2C1_SDA	I/O	1	I²C1 serial data
	CT32B3_PWM1	O	7	32-bit timer/counter 3 pulse width modulation data output 1
99	I2S_MCLK1	O	–	I²S master clock output 1
100	P4.8	I/O	D	GPIO4 pin 8
	I2C1_SCL	O	1	I²C1 serial clock
	CT32B3_PWM2	O	7	32-bit timer/counter 3 pulse width modulation data output 2
101	VDD12	P	–	1.2V power supply
102	VDD33	P	–	3.3V power supply
103	VSS	GND	–	Ground
104	P2.9	I/O	D	GPIO2 pin 9
	LCD_D1	O	1	TFT-LCD data bus
	8080_D1	O	2	8080 CPU data bus
105	P2.8	I/O	D	GPIO2 pin 8
	LCD_D0	O	1	TFT-LCD data bus
	8080_D0	O	2	8080 CPU data bus
	I2S4_WS	I/O	5	I²S4 word select

No.	Name	Type[11]	Mode[12]	Description
106	P2.7	I/O	D	GPIO2 pin 7
	LCD_DCLK	O	1	TFT-LCD clock
	8080_A0	O	2	8080 CPU address 0
	I2S4_BCLK	I/O	5	I²S4 bit clock. Bit clock can be programmed as a master or a slave.
	CT32B4_PWM2	O	7	32-bit timer/counter 4 pulse width modulation data output 2
107	P2.6	I/O	D	GPIO2 pin 6
	LCD_DE	O	1	TFT-LCD data enable
	8080_CS	O	2	8080 CPU chip select; active low
	I2S4_DOUT	O	5	I²S4 data output
	CT32B5_PWM0	O	7	32-bit timer/counter 5 pulse width modulation data output 0
108	P2.5	I/O	D	GPIO2 pin 5
	LCD_VSYNC	O	1	TFT-LCD vertical/frame synchronization
	8080_WR	O	2	8080 CPU write; active low
	I2S4_DIN	I	5	I²S4 data input
	CT32B5_PWM1	O	7	32-bit timer/counter 5 pulse width modulation data output 1
109	P2.4	I/O	D	GPIO2 pin 4
	LCD_HSYNC	O	1	TFT-LCD horizontal/line synchronization
	8080_RD	O	2	8080 CPU read; active low
	I2S4_MCLK	I/O	5	I²S4 master clock
	CT32B5_PWM2	O	7	32-bit timer/counter 5 pulse width modulation data output 2
110	P0.8	I/O	D	GPIO0 pin 8
	SPIFC_CS	O	1	SPI NOR flash chip select
	SPI0DMA_CS	O	3	SPI0 with DMA chip select
111	P1.3	I/O	D	GPIO1 pin 3
	CIS_HSYNC	I	2	CMOS image sensor output horizontal sync
	NAND_RE	O	3	NAND flash read enable
	LCD_VSYNC/ 8080_WR	O	4	TFT-LCD vertical/frame synchronization/ 8080 CPU write; active low
112	P1.2	I/O	D	GPIO1 pin 2
	CIS_VSYNC	I	2	CMOS image sensor output vertical sync
	NAND_WE	O	3	NAND flash write enable
	LCD_HSYNC/ 8080_RD	O	4	TFT-LCD horizontal/line synchronization/ 8080 CPU read; active low
113	VDD12	P	–	1.2V power supply
114	P1.13	I/O	D	GPIO1 pin 13
	CIS_D7	I	2	CMOS image sensor output data
	NAND_D7	I/O	3	NAND flash data input/output
	LCD_D7/ 8080_D7	O	4	TFT-LCD data bus/ 8080 CPU data bus
115	P1.12	I/O	D	GPIO1 pin 12
	CIS_D6	I	2	CMOS image sensor output data
	NAND_D6	I/O	3	NAND flash data input/output
	LCD_D6/ 8080_D6	O	4	TFT-LCD data bus/ 8080 CPU data bus
116	P1.11	I/O	D	GPIO1 pin 11
	CIS_D5	I	2	CMOS image sensor output data
	NAND_D5	I/O	3	NAND flash data input/output
	LCD_D5/ 8080_D5	O	4	TFT-LCD data bus/ 8080 CPU data bus
117	P1.10	I/O	D	GPIO1 pin 10
	CIS_D4	I	2	CMOS image sensor output data
	NAND_D4	I/O	3	NAND flash data input/output
	LCD_D4/ 8080_D4	O	4	TFT-LCD data bus/ 8080 CPU data bus
118	VDD12	P	–	1.2V power supply
119	P0.10	I/O	D	GPIO0 pin 10
	SPIFC_MISO	I	1	SPI NOR flash master in slave out
	SPI0DMA_MISO	I	3	SPI0 with DMA master in slave out
120	P0.0	I/O	D	GPIO0 pin 0
	I2C0_SCL	O	1	I²C0 serial clock

No.	Name	Type[11]	Mode[12]	Description
121	P0.12	I/O	D	GPIO0 pin 12
	SPIFC_D2/ SPIFC_WP	I/O	1	SPI NOR flash 4 x I/O mode, data pin or write protection
	SPI0DMA_MISO2	I	3	SPI0 with DMA master in slave out
	CT32B0_PWM1	O	7	32-bit timer/counter 0 pulse width modulation data output 1
122	P0.1	I/O	D	GPIO0 pin 1
	I2C0_SDA	I/O	1	I²C0 serial data
123	VDD33	P	–	3.3V power supply
124	VSS	GND	–	Ground
125	P3.15	I/O	D	GPIO3 pin 15
	SPI1_MOSI	I/O[13]	1	SPI1 master out slave in
	SPI1DMA_MOSI	O	4	SPI1 with DMA master out slave in
	CT32B3_CAP0	I	6	32-bit timer/counter 3 capture channel 0
	CT32B2_PWM2	O	7	32-bit timer/counter 2 pulse width modulation data output 2
126	P3.14	I/O	D	GPIO3 pin 14
	SPI1_MISO	I/O[14]	1	SPI1 master in slave out
	NAND_D7	I/O	3	NAND flash data input/output
	SPI1DMA_MISO	I	4	SPI1 with DMA master in slave out
	CT32B2_CAP0	I	6	32-bit timer/counter 2 capture channel 0
	CT32B3_PWM0	O	7	32-bit timer/counter 3 pulse width modulation data output 0
127	P3.13	I/O	D	GPIO3 pin 13
	SPI1_SCLK	I/O[13]	1	SPI1 serial clock
	NAND_D6	I/O	3	NAND flash data input/output
	SPI1DMA_SCLK	O	4	SPI1 with DMA serial clock
	CT32B1_CAP0	I	6	32-bit timer/counter 1 capture channel 0
	CT32B3_PWM1	O	7	32-bit timer/counter 3 pulse width modulation data output 1
128	P3.12	I/O	D	GPIO3 pin 12
	SPI1_CS	I/O[13]	1	SPI1 chip select
	NAND_D5	I/O	3	NAND flash data input/output
	SPI1DMA_CS	O	4	SPI1 with DMA chip select
	CT32B0_CAP0	I	6	32-bit timer/counter 0 capture channel 0
	CT32B3_PWM2	O	7	32-bit timer/counter 3 pulse width modulation data output 2

3.3.3 Pinmux

Table 3–6 Pinmux Overview for SNC73522[15]

Default	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
P0.0	I2C0_SCL	–	–	–	–	–	–
P0.1	I2C0_SDA	–	–	–	–	–	–
P0.2	UART0_TXD	–	–	–	–	–	CT32B7_PWM2
P0.3	UART0_RXD	–	–	–	–	–	CT32B7_PWM1
P0.4	AIN0	–	–	–	–	–	CT32B7_PWM0
P0.5	AIN1	–	–	–	–	–	CT32B6_PWM2
P0.6	AIN2	–	–	–	–	–	CT32B6_PWM1
P0.7	AIN3	–	–	–	–	–	CT32B6_PWM0
P0.8	SPIFC_CS	–	SPI0DMA_CS	–	–	–	–
P0.9	SPIFC_CLK	–	SPI0DMA_SCLK	–	–	–	–
P0.10	SPIFC_MISO	–	SPI0DMA_MISO	–	–	–	–
P0.11	SPIFC_MOSI	–	SPI0DMA_MOSI	–	–	–	–
P0.12	SPIFC_D2/ SPIFC_WP	–	SPI0DMA_MISO2	–	–	–	CT32B0_PWM1
P0.13	SPIFC_D3	–	SPI0DMA_MISO3	–	–	–	CT32B0_PWM0
P0.14	–	CLKOUT	–	SPI0_CS	–	–	–
P0.15	–	–	NAND_CE	SPI0_SCLK	–	–	–
P1.0	–	–	NAND_RB	SPI0_MISO	–	–	–
P1.1	–	–	NAND_ALE	SPI0_MOSI	–	–	–
P1.2	–	CIS_VSYNC	NAND_WE	LCD_HSYNC/ 8080_RD	–	–	–
P1.3	–	CIS_HSYNC	NAND_RE	LCD_VSYNC/ 8080_WR	–	–	–
P1.4	SD0_CLK	CIS_MCLK	NAND_WP	LCD_DE/ 8080_CS	SPI0DMA_CS	–	CT32B7_PWM2
P1.5	SD0_CMD	CIS_PCLK	NAND_CLE	LCD_DCLK/ 8080_A0	SPI0DMA_SCLK	–	CT32B7_PWM1
P1.6	SD0_D0	CIS_D0	NAND_D0	LCD_D0/ 8080_D0	SPI0DMA_MISO	–	CT32B7_PWM0
P1.7	SD0_D1	CIS_D1	NAND_D1	LCD_D1/ 8080_D1	SPI0DMA_MOSI	–	CT32B6_PWM2
P1.8	SD0_D2	CIS_D2	NAND_D2	LCD_D2/ 8080_D2	SPI0DMA_MISO2	–	CT32B6_PWM1
P1.9	SD0_D3	CIS_D3	NAND_D3	LCD_D3/ 8080_D3	SPI0DMA_MISO3	–	CT32B6_PWM0

[15] "–" represents reserved pinmux options.

Default	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
P1.10	–	CIS_D4	NAND_D4	LCD_D4/ 8080_D4	–	–	–
P1.11	–	CIS_D5	NAND_D5	LCD_D5/ 8080_D5	–	–	–
P1.12	–	CIS_D6	NAND_D6	LCD_D6/ 8080_D6	–	–	–
P1.13	–	CIS_D7	NAND_D7	LCD_D7/ 8080_D7	–	–	–
P1.14	SDIO_CLK	–	–	–	I2S4_MCLK	–	–
P1.15	SDIO_CMD	–	–	–	I2S4_DIN	–	–
P2.0	SDIO_D0	–	–	–	I2S4_DOUT	–	–
P2.1	SDIO_D1	–	–	–	I2S4_BCLK	–	–
P2.2	SDIO_D2	–	–	–	I2S4_WS	–	–
P2.3	SDIO_D3	–	–	–	–	–	–
P2.4	LCD_HSYNC	8080_RD	–	–	I2S4_MCLK	–	CT32B5_PWM2
P2.5	LCD_VSYNC	8080_WR	–	–	I2S4_DIN	–	CT32B5_PWM1
P2.6	LCD_DE	8080_CS	–	–	I2S4_DOUT	–	CT32B5_PWM0
P2.7	LCD_DCLK	8080_A0	–	–	I2S4_BCLK	–	CT32B4_PWM2
P2.8	LCD_D0	8080_D0	–	–	I2S4_WS	–	–
P2.9	LCD_D1	8080_D1	–	–	–	–	–
P2.10	LCD_D2	8080_D2	–	–	–	–	–
P2.11	LCD_D3	8080_D3	–	–	–	–	–
P2.12	LCD_D4	8080_D4	–	–	–	–	–
P2.13	LCD_D5	8080_D5	–	–	–	–	–
P2.14	LCD_D6	8080_D6	–	–	–	–	–
P2.15	LCD_D7	8080_D7	–	–	–	–	–
P3.0	LCD_D8	8080_D8	NAND_CE	–	–	–	–
P3.1	LCD_D9	8080_D9	NAND_RB	–	–	–	–
P3.2	LCD_D10	8080_D10	NAND_ALE	–	I2S4_MCLK	I2C2_SCL	–
P3.3	LCD_D11	8080_D11	NAND_WE	–	I2S4_DIN	I2C2_SDA	–
P3.4	LCD_D12	8080_D12	NAND_RE	–	I2S4_DOUT	I2S1_DIN	–
P3.5	LCD_D13	8080_D13	NAND_WP	SD0_CLK	I2S4_BCLK	I2S1_BCLK	–
P3.6	LCD_D14	8080_D14	NAND_CLE	SD0_CMD	I2S4_WS	I2S1_WS	–
P3.7	LCD_D15	8080_D15	NAND_D0	SD0_D0	–	I2S3_DOUT	–
P3.8	LCD_D16	–	NAND_D1	SD0_D1	–	I2S3_BCLK	–
P3.9	LCD_D17	–	NAND_D2	SD0_D2	–	I2S3_WS	–
P3.10	–	–	NAND_D3	SD0_D3	–	–	CT32B4_PWM1
P3.11	–	–	NAND_D4	–	–	–	CT32B4_PWM0
P3.12	SPI1_CS	–	NAND_D5	SPI1DMA_CS	–	CT32B0_CAP0	CT32B3_PWM2
P3.13	SPI1_SCLK	–	NAND_D6	SPI1DMA_SCLK	–	CT32B1_CAP0	CT32B3_PWM1
P3.14	SPI1_MISO	–	NAND_D7	SPI1DMA_MISO	–	CT32B2_CAP0	CT32B3_PWM0

Default	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
P3.15	SPI1_MOSI	–	–	SPI1DMA_MOSI	–	CT32B3_CAP0	CT32B2_PWM2
P4.0	UART1_TXD	–	–	SPI1DMA_MISO2	–	CT32B4_CAP0	CT32B2_PWM1
P4.1	UART1_RXD	–	–	SPI1DMA_MISO3	–	CT32B5_CAP0	CT32B2_PWM0
P4.2	AIN4	–	–	–	–	CT32B6_CAP0	CT32B1_PWM2
P4.3	AIN5	–	–	–	–	CT32B7_CAP0	CT32B1_PWM1
P4.4	–	–	–	–	–	–	CT32B1_PWM0
SWO	P4.5	–	–	–	–	–	CT32B0_PWM2
SWCLK	P4.6	–	–	–	–	–	CT32B0_PWM1
SWDIO	P4.7	–	–	–	–	–	CT32B0_PWM0
P4.8	I2C1_SCL	–	–	–	–	–	CT32B3_PWM2
P4.9	I2C1_SDA	–	–	–	–	–	CT32B3_PWM1
P4.10	I2S0_DIN	–	–	–	–	–	CT32B3_PWM0
P4.11	I2S0_BCLK	–	–	–	–	–	CT32B2_PWM2
P4.12	I2S0_WS	CIS_D4	–	–	–	–	–
P4.13	I2S2_DOUT	CIS_D5	–	–	–	–	–
P4.14	I2S2_BCLK	CIS_D6	–	–	–	–	–
P4.15	I2S2_WS	CIS_D7	–	–	–	–	–

4 Central Processing Unit (CPU)

4.1 Dual-core Architecture

The SNC7352x series integrates two ARM Cortex-M3 processors, Core 0 and Core 1. Both cores can access the 256 KB shared AHB RAM, 4 KB mailbox RAM, and all peripherals. The Core 0 takes the role of a master core which controls the operation mode of the system and boots the code of Core 1. The Core 1 acts as a slave core, and is an independent subsystem. Two cores interact by the inter-process communication (IPC) protocol. The most important function of the two cores is to separate two subsystems of the SNC7352x series, not only to increase the performance of the system, but also to reduce the code complexity of each core.

4.1.1 ARM Cortex-M3 Processor

The ARM Cortex-M3 is a low-power processor that features low gate count, low interrupt latency, and low-cost debugging. It is intended for embedded applications requiring fast interrupt response features. The processor implements the ARM architecture v7-M. The processor incorporates:

- Memory Protect Unit (MPU)
- Nested Vectored Interrupt Controller (NVIC)
- Serial wire debug (SWD) port with Trace Port Interface Unit (TPIU) and Data Watchpoint and Trace (DWT) debug protocol

For complete details on the ARM Cortex-M3, please refer to the technical reference manual available at https://www.arm.com/products/silicon-ip-cpu/cortex-m/cortex-m3.

4.1.2 Inter-processor Communication (IPC)

The communication between the two cores is achieved with IPC which is implemented with a ring buffer of software framework. Messages are passed through queues using a cyclic share buffer as message box RAM (0x2000_0000 to 0x2000_0FFF). A queue is filled with message boxes from start to end addresses. Two cores use these share RAM to inter-change data and commands.

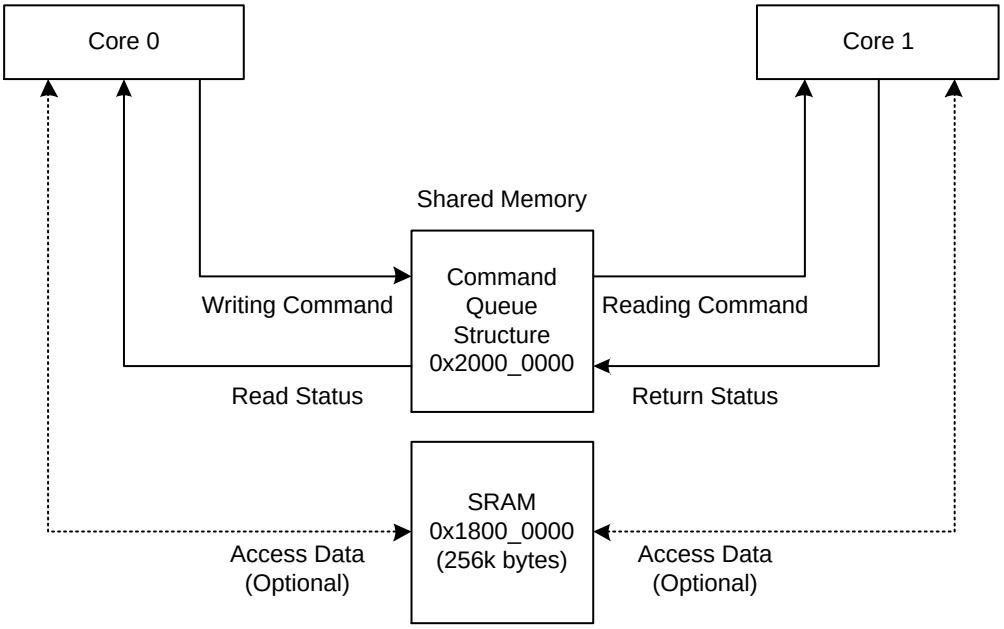


Figure 4–1 Inter-processor Communication Block Diagram

4.2 Memory Protect Unit (MPU)

The Memory Protect Unit (MPU) is a component for memory protection of the SNC7352x series. The processors support the standard ARMv7 Protected Memory System Architecture model.

Features of the MPU include:

- Protection regions
- Overlapping protection regions with ascending region priority
  - 7 = Highest priority
  - 0 = Lowest priority
- Access permissions
- Exporting memory attributes to the system

The MPU mismatches and permission violations invoke the programmable-priority MemManage fault handler. For more information, see the ARMv7-M Architecture Reference Manual.
Major functions of the MPU include:

- Enforce privilege rules
- Separate processes
- Enforce access rules

Please refer to the official website of ARM for more details:
https://developer.arm.com/documentation/dui0552/a/cortex-m3-peripherals/optional-memory-protection-unit?lang=en

4.3 Nested Vectored Interrupt Controller (NVIC)

The nested vectored interrupt controller (NVIC) provides a software interface to the interrupt system. Based on the ARM subsystem, the SNC7352x series has one level of interrupts: Interrupt Request (IRQ) for general interrupts.

The sequence of events for the interrupts is:

1. INTC collects interrupt signals from various modules
2. INTC generates the IRQ interrupt signals to the ARM

The properties of all interrupt signals can be configured by the INTC registers which are mapped to the AHB peripherals. The INTC supports up to 57 interrupt sources. The software initializes edge or level sensitivity and checks the source of the interrupt when it receives IRQ events from the ARM. The registers of INTC are at base address 0xE000_E000.

Features of the NVIC are:

- Up to 64 vectored interrupts
- Programmable priority levels of 0–7 for each interrupt. Higher levels correspond to a lower priority. Thus, level 0 is the highest interrupt priority with low-latency exception for interrupt handling.
- Level and pulse detection of interrupt signals
- Dynamic reprioritization of interrupts
- Grouping of priority values into group priority and sub-priority fields
- Interrupt tail-chaining
- External non-maskable interrupt (NMI)

Please refer to the official website of ARM for more details:
https://developer.arm.com/documentation/100166/0001/Nested-Vectored-Interrupt-Controller?lang=en

4.4 System Clock

The system clock is the major clock domain except for the USB and the WDT. A divider is used to lower the operating clock for all IPs in the system clock domain. The CPU uses the 12 MHz internal high-speed RC (IHRC) as the default system source clock for boot up. The source of the system clock is configurable for better performance or power saving. The system clock block diagram is as shown in Figure 4–2, and Table 4–1 lists the sources of the system clock.

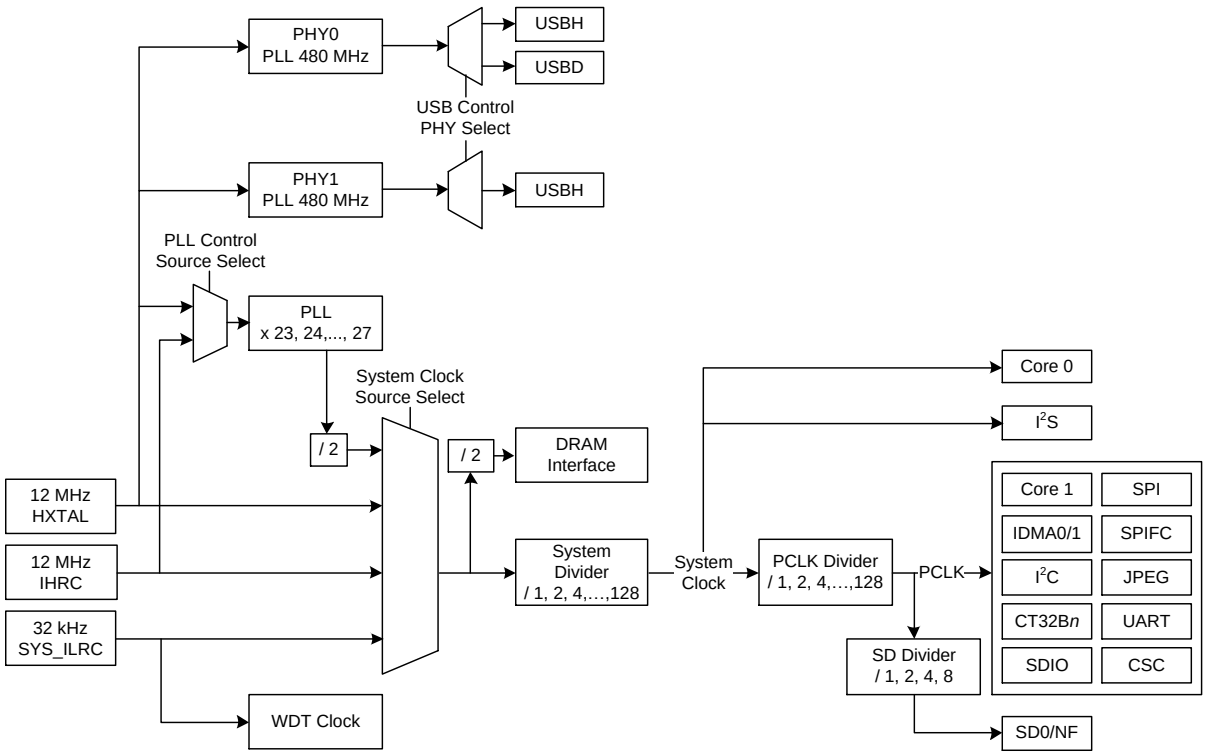


Figure 4–2 System Clock Block Diagram

Table 4–1 Sources of System Clock

Source	Frequency	Interface	Default	Note
IHRC	12 MHz	Internal	On	Power on default (±2% tolerance)
HXTAL	12 MHz	External: HXIN/HXOUT	Off	–
SYS_ILRC	32 kHz	–	On	Always on
PLL	276–324 MHz	Internal	Off	System Clock = PLL / 2

4.4.1 Phase-Locked Loops (PLL)

Features of the PLL are:

- Provides primary system clock
- Programmable PLL divider value
- Programmable PLL multiplier value
- Accepts IHRC input or HXTAL input

The PLL module requires one primary reference clock. The reference 12 MHz clock frequency may be generated either by the IHRC or the HXTAL. The SNC7352x series has two sets of PLL for the system and the USB.

Table 4–2 PLL Clock Frequency

Module	Output Frequency	Description
System PLL	276–324 MHz	For main system clocks (12 MHz HXTAL/IHRC x 23, 24,…, 27)
USB_PLL	480 MHz	For USB host and device

Table 4–3 PLL List

Name	Used by	Maximum Frequency
System Clock	CPU0/CPU1	162 MHz
	AHB	162 MHz for the ROM, the SRAM, and the IP blocks on AHB including the peripherals
System Clock / 2	DRAM	81 MHz
PLL	USB device	480 MHz
	USB host	480 MHz
ILRC (1.2V)	WDT	32 kHz

4.5 Hardware Accelerators

Comparing to processing with pure software, fast Fourier transform (FFT) and finite impulse response (FIR), the hardware accelerators of Core 1 require less instruction cycles when handling audio and image related algorithms.

Features of the FIR accelerator are:

- 16-bit input and 32-bit output data width
- Data overflow handling
- Programmable FIR tap (max. 2048)
- Suitable for algorithms including but not limited to acoustic echo cancellation, equalizer, 3D audio speech codec, and image enhancement

Features of the FFT accelerator are:

- 16-bit input and 32-bit output data width
- Data overflow handling
- Programmable FFT tap (max. 1024)
- Suitable for algorithms including but not limited to voice recognition, sound effect, and fingerprint identification

5 Memory

5.1 Physical Memory Map

The SNC7352x series provides private libraries such as the USB library and FAT system to save memory size. There are 64 KB in the internal ROM, and there is a 64 KB PRAM dedicated for CPU programs for Core 0. Furthermore, a 256 KB internal memory is equipped to be shared by the CPU and peripherals. A ROM is dedicated for digital signal processing programs of Core 1.

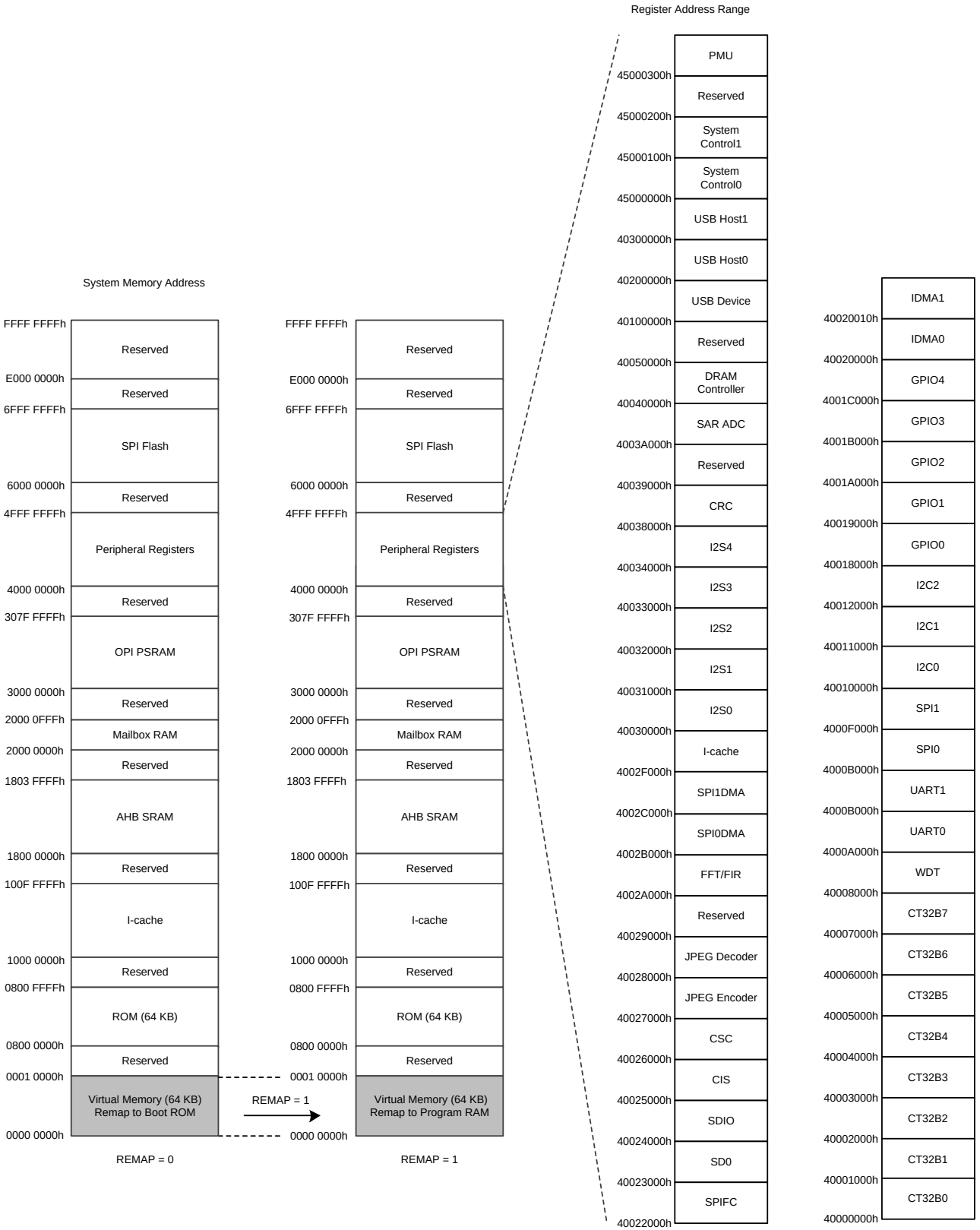


Figure 5–1 Memory Map

Table 5–1 Internal Memory

Region	Internal RAM Address Range	Size	Access		
			Core 0	Core 1	Peripheral DMAs
ROM (Core 0)	0x0800_0000–0x0800_FFFF	64 KB	R	–	–
Program RAM	0x0000_0000–0x0000_FFFF (After remap)	64 KB	R	–	–
ROM (Core 1)	0x0000_0000–0x0001_FFFF	128 KB	–	R	–
I-cache	0x1000_0000–0x100F_FFFF	1 MB	R	R	–
AHB SRAM	0x1800_0000–0x1803_FFFF	256 KB	R/W	R/W	R/W
Mailbox RAM	0x2000_0000–0x2000_0FFF	4 KB	R/W	R/W	–

Table 5–2 External Memory

Region	External Memory Address Range	Size	Access		
			Core 0	Core 1	Peripheral DMAs
OPI PSRAM	0x3000_0000–0x307F_FFFF	8 MB	R/W	R/W	R/W[16]
SPI NOR flash	0x6000_0000–0x6FFF_FFFF	256 MB	R	R	R/W[16]

5.2 DMA Controller

The DMA controller controls data transfer between the modules as listed in Table 5–3, along with SRAM access. There are a total of 19 sets of DMA channels where each channel functions independently. 17 sets function for a designated IP, and DMA0 and DMA1 are for general purpose.

Table 5–3 DMA Channels

Module	Access to DRAM Controller (OPI PSRAM)
DMA0	Yes
DMA1	Yes
DMA-SPIFC	No
DMA-SD0/NF	No
DMA-SDIO	No
DMA-CIS	Yes
DMA-CSC-IN	No
DMA-CSC-OUT	No
DMA-JPEG_ENC-IN	No
DMA-JPEG_ENC-OUT	Yes
DMA-JPEG_DEC-IN	Yes
DMA-JPEG_DEC-OUT	No
DMA-SPI0	No
DMA-SPI1	No
DMA-I2S0	No
DMA-I2S1	No
DMA-I2S2	No
DMA-I2S3	No

[16] For certain DMAs

5.3 SPI NOR Flash Controller (SPIFC)

Features of the SPI NOR flash controller (SPIFC) include:

- Built-in SPI interface
- DMA for large data transfers
- 1/2/4-bit read mode and 1/4-bit write mode
- Supports direct addressing for CPU
- Supports MXIC/SST/GD command series serial flash

The SPI NOR flash controller block diagram is as shown in Figure 5–2.

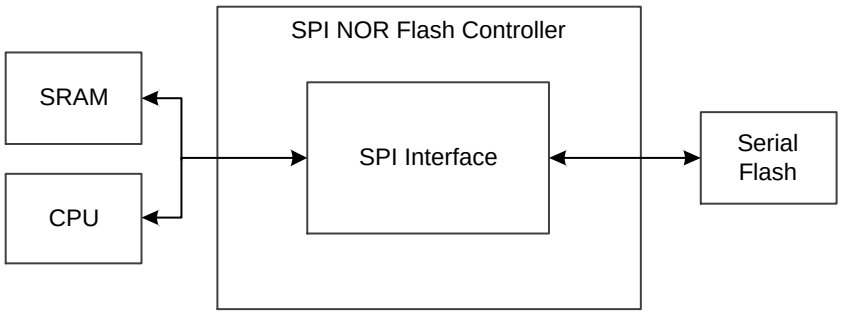


Figure 5–2 SPI NOR Flash Controller Block Diagram

5.3.1 Timing

Table 5–4 lists the switching characteristics over the condition that SPI NOR flash clock = 162 / *n* MHz where *n* = 4.

Table 5–4 Switching Characteristics for SPI NOR Flash Controller

No.	Parameter		Device			Unit
			MIN.	TYP.	MAX.	
1	$t_{c(CLK)}$	Cycle time, SPI NOR flash clock	25	–	200	ns
2	$t_{w(CLKH)}$	Pulse width, SPI NOR flash clock high	9	–	0.45P[17]	
3	$t_{w(CLKL)}$	Pulse width, SPI NOR flash clock low	9	–	0.45P[17]	
4	$t_{d(CLK-SDX)}$	Delay time, SPI NOR flash clock transmit falling edge to SF_MO data output	3	–	–	
5	$t_{oh(CLK-SDX)}$	Output hold time, SF_MO data valid after receive rising edge of clock	11	–	–	
6	$t_{d(CSN-CLK)}$	Delay time, SPI NOR flash chip select asserting to the first SPI NOR flash clock rising edge	10	–	–	
7	$t_{d(CLK-CSN)}$	Delay time, the final SPI NOR flash clock falling edge to SPI NOR flash chip select de-asserting	4	–	–	

[17] P = SF clock period

Table 5–5 Input Timing Requirements of Controller in Master Mode

No.	Parameter		Device			Unit
			MIN.	TYP.	MAX.	
8	$t_{su(SDR-CLK)}$	Setup time, SF_MI data valid before receive rising edge of SPI NOR Flash clock	4	–	–	ns
9	$t_{h(CLK-SDR)}$	Hold time, SF_MI data valid after receive rising edge of SPI NOR flash clock	11	–	–	

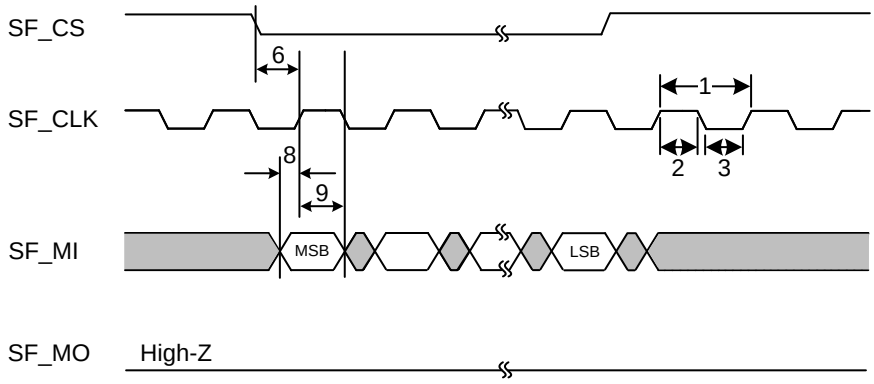


Figure 5–3 SPI NOR Flash Master Mode Input Timing

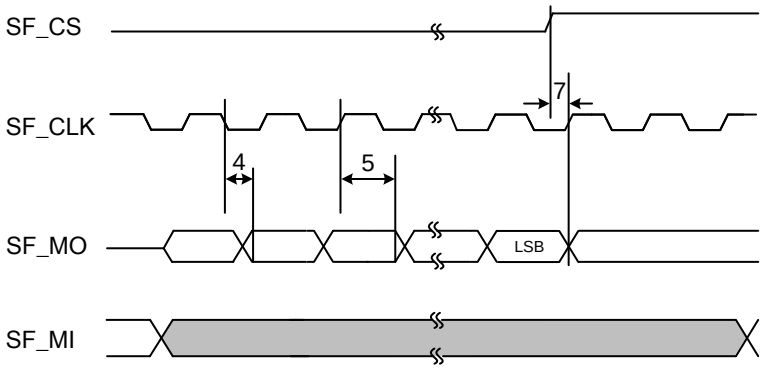


Figure 5–4 SPI NOR Flash Master Mode Output Timing

5.4 DRAM Controller

The DRAM controller has four channels for DMA or CPU access to extend the memory buffer. This controller supports pseudo SRAM (PSRAM) interface with 8-bit OPI data width.

Features of the DRAM controller are:

- Supports WRAP transfer
- AHB 32-bit data width
- Three configurable channels (0–2)
- Group round-robin arbitration scheme
- Low-power bitrate control (BRC) mode for address mapping
- Sequential DRAM burst type
- Supports auto refresh and self refresh
- Supports dynamic frequency change
- Supports OPI interface

The figure below shows DMA controller channels.

- Channel0 to Channel2: JPEG_E, JPEG_D, IDMA0/IDMA1, CIS, USB Device, USB Host0, USB Host1
- Channel3: Core 0, Core 1

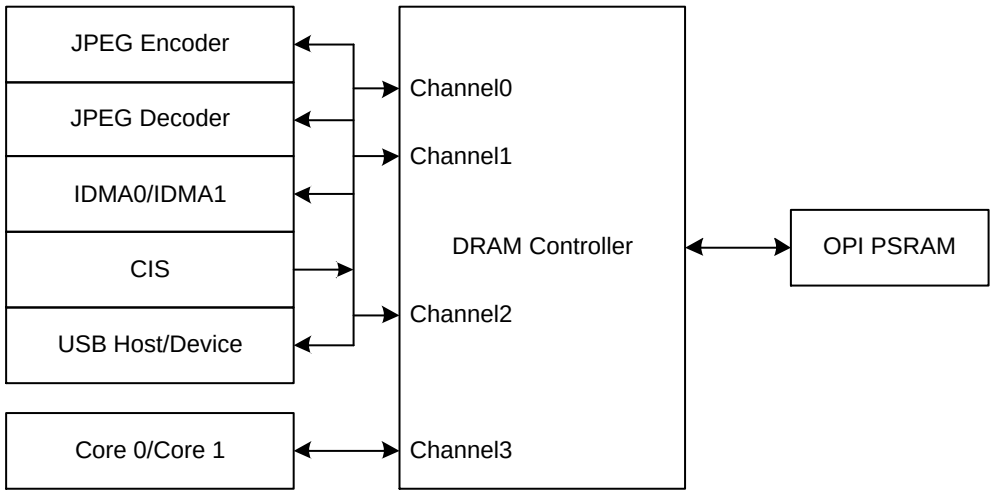


Figure 5–5 DMA Controller Channels

5.5 I-cache Controller

The SNC7352x series supports I-cache with 16 KB SRAM to correspond to 1 MB program size running at maximum clock frequency.

Features of the I-cache are:

- 64-way set-associative cache with 16 KB SRAM, 32 bytes per line
- 1 MB address mapping
- Supports OPI PSRAM or SPI flash at one time
- Supports one of the Core 0 and Core 1 at a time
- Read OPI PSRAM with burst eight transfer (32 bytes)

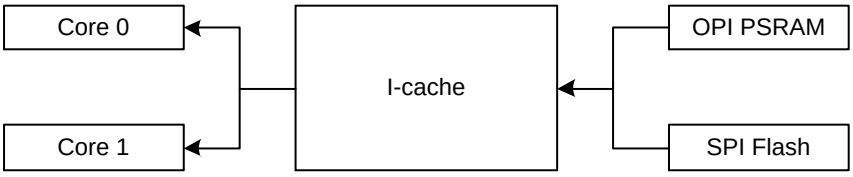


Figure 5–6 I-cache Block Diagram

Table 5–6 Throughput of DRAM Controller

DRAM Type Operating in 80 MHz	Access Unit		Read (MB/s)	Write (MB/s)
	Burst Type	Byte Per Transfer		
OPI PSRAM	Single access	4	16.4	149
	Burst4	16	49.5	149
	Burst8	32	74.9	149
	Burst16	64	100.9	149

5.6 Storage

5.6.1 SD Card Controller (SD0)

Features of the SD card controller (SD0) include:

- Built-in SD controller in 4-bit mode
- Compliant with SD 2.0 specification
- Programmable clock frequency
- Auto multiple block read/write command
- CRC-16 for the SD data
- CRC-7 for the SD command

Refer to 7.8.1 Timing of SD/SDIO Controller (SD1).

5.6.2 NAND Flash Controller

Features of the NAND flash controller include:

- SLC NAND flash
- 1/4/8-bit ECC
- 512 bytes/2 KB/4 KB page size
- DMA access

I. Timing

Table 5–7 Timing Requirements for NAND Flash Controller

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	t_{CLS}	CLE set up time	50	–	ns
2	t_{CLH}	CLE hold time	17	–	
3	t_{CS}	CE set up time	50	–	
4	t_{ALS}	ALE set up time	58	–	
5	t_{ALH}	ALE hold time	48	–	
6	t_{DS}	Data set up time	45	–	
7	t_{DH}	Data hold time	45	–	

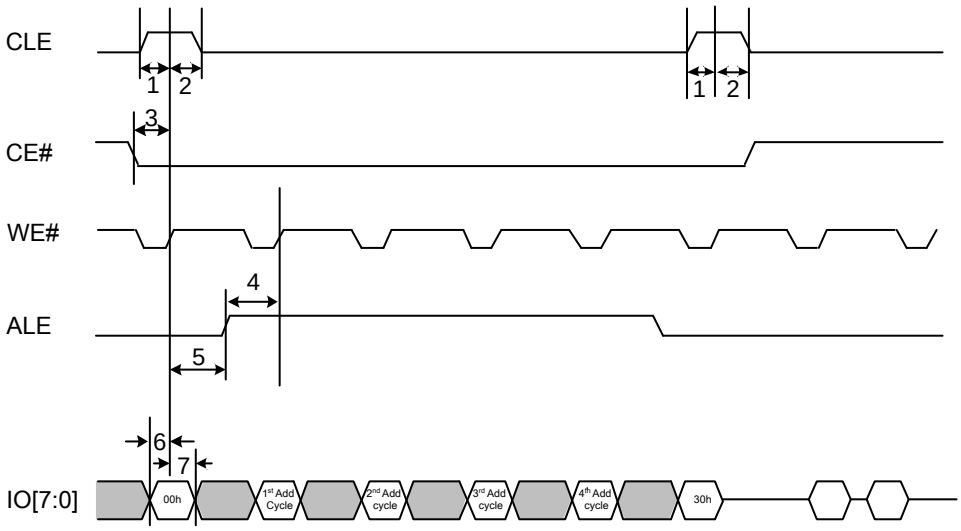


Figure 5–7 NAND Flash Controller Timing

6 System Control

6.1 System Control (SYS0/SYS1)

The system control enables the device to provide a customized solution by enabling/disabling each IP. It is easy to find a balance between high performance and low power consumption through different settings.

Features of the system control are:

- Operation modes and wakeup selection
- Change settings of the PLL and clock rate control for operation in different clock frequencies
- Disable the peripheral clocks by the clock gating registers
- Select pinmux functions and setting pull-up/down

6.2 Power Management Unit (PMU)

The SNC7352x series operates in four modes for different clock rates and power saving conditions.

- Normal mode: Core 0 and Core 1 operate, and Core 0 controls the clock system.
- Deep sleep mode: Core 0, Core 1, and all clocks besides RTC are stopped.
- Deep power-down (DPD) mode: Core 0, Core 1, SRAM, RTC (optional), and registers are powered off.

These modes control oscillators, the op-code operation, and the operation of analog peripheral devices. All of the GPIOs are switched into input-floating in deep power-down mode.

6.3 System Reset

A system reset is generated when one of the following events occurs.

- Power-on reset
  - 0.8V core power LVR trigger
  - Reset pin trigger
  - Restart program from ROM after the reset signal releases
- Low voltage reset (LVR)
  - 0.8V for core (deep sleep/DPD mode)
  - 0.95V for core (normal mode)
  - 1.8V for I/O (power-on/power-off)
  - 2.1V for I/O (normal mode)
  - Restart program from ROM after the reset signal releases
- RST pin (external reset)
  - One or two I/O power trigger
  - Restart program from ROM after the reset signal releases
- DPD wakeup reset
  - When waking up from DPD mode, the system resets and restarts from ROM
- WDT reset
  - Reset and restart program from ROM
- Software reset
  - Reset and restart from PRAM

6.4 Boot

The SNC7352x series supports several storage devices to boot up from:

- SPI NOR flash
- SD card 0
- SD card 1
- SLC NAND flash
- SPI NAND flash

After power on, the CPU searches each device for an identifying data mark and enters USB-ISP mode if the identifying data mark is not found.

In normal conditions, the CPU reads data out from the SPI NOR flash (or other storage devices). After parsing a specific data structure called the load table, the CPU places the user code to the internal-memory-address zero, which is also called PRAM, and issues a software system reset to reboot itself to the user code.

7 Peripherals

7.1 General Purpose Input/Output (GPIO)

The general-purpose input/output (GPIO) is used to transmit signals between systems and devices. GPIO pins can be configured as input, output, or interrupt input. As an output, the state driven on the output pin is controlled by writing to an internal register. As an input, the state of the input is detected by reading the state of an internal register. The GPIO supports rising edge, falling edge, both-edges, and high level/low level interrupt sense types. The SNC7352x series provides up to 80 GPIO pins in a pinmux architecture.

The options of the on-chip resistor configuration are pull-up enabled and inactive (no pull-up/pull-down by default). The repeater mode automatically enables the pull-up resistor if the pin is at logic high and enables the pull-down resistor if the pin is at logic low. Such characteristic causes the pin to retain its last known state if it is configured as an input and is not driven externally. State retention is not applicable in the deep power-down mode. The repeater mode is typically used to prevent a pin from floating and potentially using significant power if it floats to an indeterminate state when it is temporarily not driven.

Features of the GPIO include:

- Each pin triggers the GPIO interrupt independently
- The interrupt generation of each pin is triggered by rising/falling edge, both edges, or high/low level
- Each pin can be inactive, pulled high or pulled down
- A pull-up/pull-down resistor is 38 kΩ
- Output data bits can be set or cleared independently
- All pins are set to input mode at hardware reset

The GPIOs generate CPU interrupts in different interrupt/event generation modes while providing generic connections to external devices.

7.1.1 Timing

Table 7–1 and Figure 7–1 are the timing and switching characteristics over recommended operating conditions and under firmware control for GPIO.

Table 7–1 Switching Characteristics for GPIO

No.	Parameter		Device[18]		Unit
			MIN.	MAX.	
1	$t_{w(GPIH)}$	Pulse duration, GPO*n*–15 high	6.1	–	ns
2	$t_{w(GPIL)}$	Pulse duration, GPO*n*–15 low	6.1	–	

NOTE In reality, the speed of the firmware control is not fast enough to toggle GPIO in every PCLK cycle[19], and the performance of the GPIO may be affected by the PCB layout and the circuit signal length.

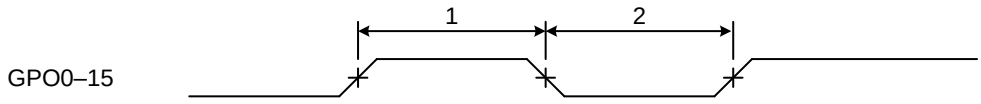


Figure 7–1 GPIO Port Timing under Firmware Control

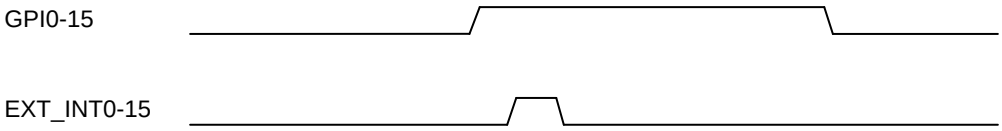


Figure 7–2 GPIO External Interrupt in Rising Edge Trigger Mode

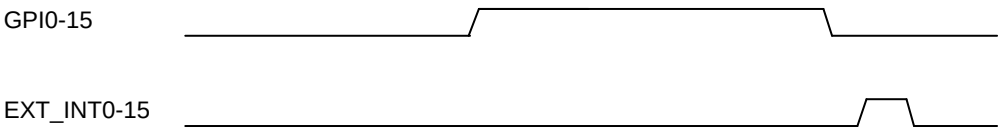


Figure 7–3 GPIO External Interrupt in Falling Edge Trigger Mode

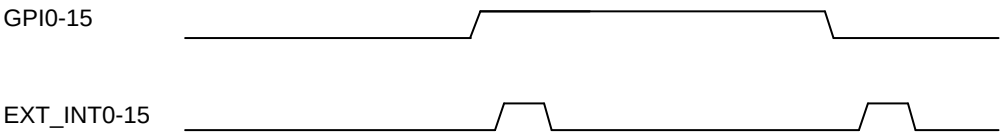


Figure 7–4 GPIO External Interrupt in Both Edges Trigger Mode

[18] The parameter value should not be used as a maximum performance specification. Actual performance of back-to-back accesses of the GPIO is dependent upon internal bus activity.
[19] Peripheral clock (PCLK) cycle = AHB peripherals clock period

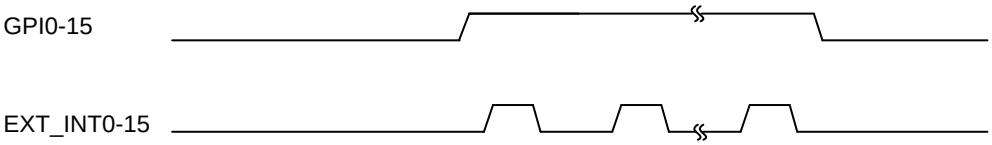


Figure 7–5 GPIO External Interrupt in High Level Trigger Mode

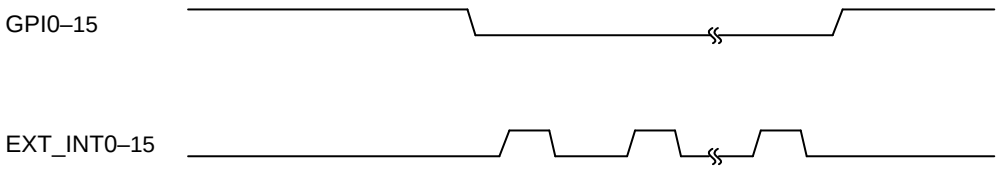


Figure 7–6 GPIO External Interrupt in Low Level Trigger Mode

7.2 Inter-integrated Circuit (I²C)

The inter-integrated circuit (I²C) interface implements the standard I²C master/slave functions and complies with the Philips I²C bus protocol. It serves as a standard master I²C device to receive/transmit data from/to a slave device over the I²C bus. On the contrary, it can also serve as a slave to respond to requests. The I²C is a two-wire bi-directional serial bus that provides a simple and efficient method of data exchange while minimizing the interconnection requirements between devices. The I²C interface is mainly used for controlling external I²C devices.

The SNC7352x series I²C is allowed to communicate with external I²C devices. The interface has two pins, serial clock (SCL) and serial data (SDA). It supports bit rates of up to 400 kbps. The SNC7352x series I²C has up to three sets of I²C controllers, I²C0, I²C1, and I²C2.

Features of the I²C include:

- I²C master
  - Standard speed up to 100 kHz
  - Fast speed up to 400 kHz
  - Start and stop generation
  - Fast mode plus up to 1 MHz
- I²C slave
  - Transmit and receive
  - Programmable I²C address detection
  - Optional recognition of up to four distinct slave addresses
  - Supports FIFO mode
  - Stop bit detection
- Arbitration handled between simultaneously transmitting masters without corruption of serial data on the bus
- Programmable clock allowing adjustment of I²C transfer rates
- Bidirectional data transfer between masters and slaves
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization as a handshake mechanism to suspend and resume serial transfer
- Generation and detection of 7-bit addressing and general call

7.2.1 Clock Ratios and Timing

According to the standard I²C protocol, the start signal, Start, is a special signal sent by the master on the bus to wake up all the slaves and indicates the start of a data transfer. The 7-bit I2C slave address (slave address + W/R) refers to the first data packet sent by the master after a start condition. It has seven slave address bits and one read/write bit. The equation for clock ratios is:

SCL High Period Time = (SCLH+1) * I2Cn_PCLK cycle
SCL Low Period Time = (SCLL+1) * I2Cn_PCLK cycle

The slave mode is used to transmit or receive data based on the address information. After receiving the slave address successfully, the corresponding slave pulls down the SDA at the ninth SCL cycle and returns an acknowledgement signal (ACK) to the master. Then, a subsequent data transfer can start. The data transfer "DATA" refers to data receive/transmit according to read/write commands after the master receives the slave address ACK signal successfully. During the data transfer, the SDA changes its state only when the SCL is low. The SDA holds when the SCL is high. Each time the receiver gets one byte, it must send an ACK signal to the transmitter. The transmitter stops or restarts the data transfer when it does not receive the ACK signal.
The stop signal, Stop, is a special signal sent by the master to indicate the end of the data transfer according to the I²C protocol. It occurs when the transfer is complete and there are no subsequent transfers required. Once the master sends the stop signal, the slave must release the bus.

Table 7–2 Timing Requirements for I²C

No.	Parameter		Device				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
1	$t_{c(SCL)}$	Cycle time, SCL	10	–	2.5	–	µs
2	$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7	–	0.6	–	
3	$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4	–	0.6	–	
4	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7	–	1.3	–	
5	$t_{w(SCLH)}$	Pulse duration, SCL high	4	–	0.6	–	
6	$t_{su(SDAV-SCLH)}$	Setup time, SDA valid before SCL high	250	–	100	–	
7	$t_{h(SDA-SCLL)}$	Hold time, SDA valid after SCL low	0	3.45	0	0.9	
8	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7	–	1.3	–	
9	$t_{r(SDA)}$	Rise time, SDA	–	1000	$20 + 0.1C_b$[20]	300	ns
10	$t_{r(SCL)}$	Rise time, SCL	–	1000	$20 + 0.1C_b$	300	
11	$t_{f(SDA)}$	Fall time, SDA	–	300	$20 + 0.1C_b$	300	
12	$t_{f(SCL)}$	Fall time, SCL	–	300	$20 + 0.1C_b$	300	
13	$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4	–	0.6	–	µs
14	$t_{w(SP)}$	Pulse duration, spike (must be suppressed)	–	–	–	50	
15	C_b	Capacitive load for each bus line	–	400	–	400	pF

[20] Cb = total capacitance of one bus line in pF. Faster fall-times are allowed when mixing with HS-mode devices.

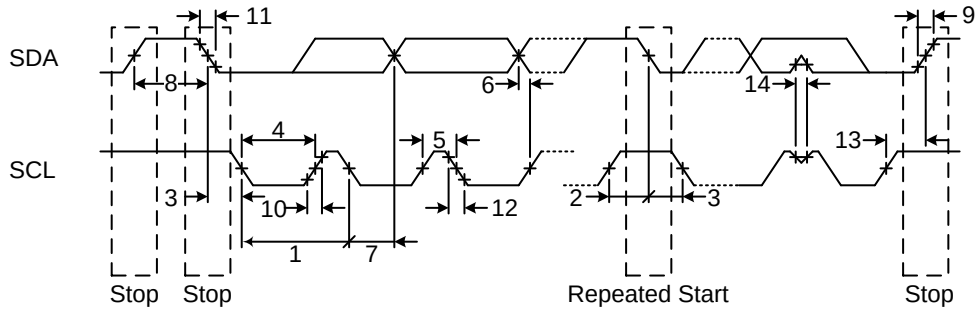


Figure 7–7 I²C Receive Timings

Table 7–3 Switching Characteristics for I²C

No.	Parameter		Device				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
16	$t_{c(SCL)}$	Cycle time, SCL	10	–	2.5	–	µs
17	$t_{d(SCLH-SDAL)}$	Delay time, SCL high to SDA low (for a repeated START condition)	4.7	–	0.6	–	
18	$t_{d(SDAL-SCLL)}$	Delay time, SDA low to SCL low (for a START and a repeated START condition)	4	–	0.6	–	
19	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7	–	1.3	–	
20	$t_{w(SCLH)}$	Pulse duration, SCL high	4	–	0.6	–	
21	$t_{d(SDAV-SCLH)}$	Delay time, SDA valid to SCL high	250	–	100	–	
22	$t_{v(SCLL-SDAV)}$	Valid time, SDA valid after SCL low (For I²C devices)	0	–	0	0.9	
23	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7	–	1.3	–	
24	$t_{d(SCLH-SDAH)}$	Delay time, SCL high to SDA high (for STOP condition)	4	–	0.6	–	
25	C_p	Capacitance for each I²C pin	–	10	–	10	

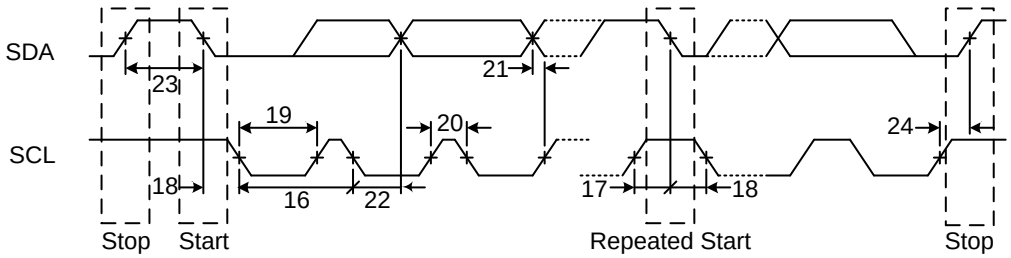


Figure 7–8 I²C Transmit Timings

7.2.2 Arbitration and Synchronization Logic

In the master transmitter mode, the arbitration logic checks that every transmitted logic 1 actually appears as a logic 1 on the I^2C bus. If another device on the bus overrules a logic 1 and pulls the SDA line low, the arbitration is lost, and the I^2C block immediately changes from master transmitter to slave receiver. The I^2C block will continue to output clock pulses on SCL until transmission of the current serial byte is complete.

Arbitration may also be lost in the master receiver mode. Loss of arbitration in this mode only occurs when the I^2C block returns a “not acknowledge” message to the bus. Arbitration is lost when another device on the bus pulls this signal low. Since this occurs only at the end of a serial byte, the I^2C block generates no further clock pulses.

7.3 Serial Peripheral Interface (SPI)

The SPI interface is a 4-wire interface where the SSEL signal behaves as a slave select. The main feature of the SPI format is that the inactive state and phase of the SCK signal are programmable through the CPOL and CPHA bits in SPI*n*_CTRL1 register. When the “CPOL” clock polarity control bit is LOW, it produces a steady state low value on the SCK pin.

If the CPOL clock polarity control bit is HIGH, a steady state high value is placed on the CLK pin when data is not being transferred. The CPHA clock phase bit controls the phase of the clock on which data is sampled. When CPHA = 1, the first edge of SCK is for data transition, and receive and transmit data is at the second edge of the SCK. When CPHA = 0, the first bit is fixed already, and the first edge of the SCK is to receive and transmit data. When the SPI is in master mode, it has to connect with one slave device as shown in Figure 7–9.

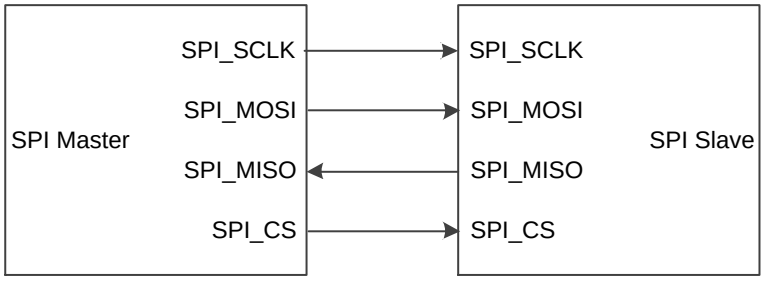


Figure 7–9 SPI Connection Diagram

The SPI controller interacts with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. Data transfers are in principle full duplex, with frames of 4 to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice it is often the case that only one of these data flows carries meaningful data.

Features of the SPI include:

- Compatible with Motorola SPI, and 4-wire TI SSI bus.
- Synchronous Serial Communication.
- Supports master or slave operation.
- 8-frame FIFO for both transmitter and receiver.
- 4-bit to 16-bit frame.
- Maximum SPI speed of 40.5 MHz in master mode or 40.5 MHz in slave mode
- Data transfer format is from MSB or LSB controlled by register
- The start phase of data sampling location selection is first phase or second phase controlled register

7.3.1 Clock Ratios and Timing

When the SPI controller is in master mode, the frequency of SCLK_OUT is derived from the following equation:

$$F_{SCLK} = F_{SPICLK}^{21} / (2 \times (SCLKDIV + 1))$$

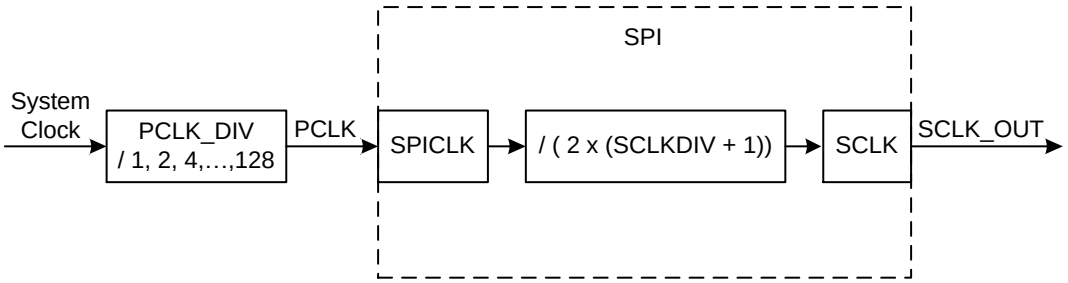


Figure 7–10 SPI Clock Block Diagram

The bit rate of the SPI is the frequency of the SCLK_OUT which is controlled by SPI_SCLKDIV in the clock divide register. When the SPI controller is in slave mode, SCLKDIV is ignored, and the SPI transfer bitrate is decided on the master side. Due to clocks synchronization, the bit clock from the master side has to be slower than SPICLK by at least six times.

SCLK stops toggling when it is idling. The frame/sync is used as the chip-select signal. Through the SPI interface, data is transmitted and received simultaneously to and from an external device. The data lines are synchronized by a serial clock.

In master mode, when the SPI controller is enabled and TX FIFO contains data, the transmit logic reads the data in TX FIFO and shifts it out at every transmit edge (depending on SCLKPO and SCLKPH) from MSB to LSB. Synchronously, the receive logic receives data. After the LSB is transmitted or received, frame/sync holds low for half or one SCLK cycle, depending on SCLKPH, and then pulled high if TX FIFO is empty. Received data is written into RX FIFO. When TX FIFO is not empty, the transmit logic restarts to transmit data.

In slave mode, when frame/sync is activated and SCLK is enabled, the transmit logic tries to shift the data into the TX FIFO even if the TX FIFO is empty. The transmit FIFO under-run interrupt is issued when TX FIFO is enabled. The receive logic receives data at the same time, and the data is written into RX FIFO.

Table 7–4 Input Timing Requirements for SPI in Master Mode

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	$t_{su(RX-CLK)}$	Setup time, SPI_MOSI valid before receive rising or falling edge of SPI_SCLK	10	–	ns
2	$t_{h(CLK-RX)}$	Hold time, SPI_MOSI valid after receive rising or falling edge of SPI_SCLK	15	–	

Table 7–5 Switching Characteristics for SPI in Master Mode

No.	Parameter		Device		Unit
			MIN.	MAX.	
3	$t_{c(CLK)}$	Cycle time, SPI_SCLK	25	–	ns
4	$t_{w(CLKH)}$	Pulse width, SPI_SCLK high	0.45 ($t_{c(CLK)}$)	–	
5	$t_{w(CLKL)}$	Pulse width, SPI_SCLK low	0.45 ($t_{c(CLK)}$)	–	

[21] $F_{SPICLK} = F_{PCLK}$

No.	Parameter		Device		Unit
			MIN.	MAX.	
6	$t_{osu(TX-CLK)}$	Ouput setup time, SPI_MISO valid before initial SPI_SCLK rising or falling edge.	0.5 ($t_{c(CLK)}$) - 4	–	ns
7	$t_{d(CLK-TX)}$	Delay time, SPI_SCLK transmit rising or falling edge to SPI_MISO output	4	–	
8	$t_{oh(CLK-TX)}$	Output hold time, SPI_MISO valid after receive rising or falling edge of SPI_SCLK	0.5 ($t_{c(CLK)}$) - 4	–	

The SPI data transfer timings are as below:

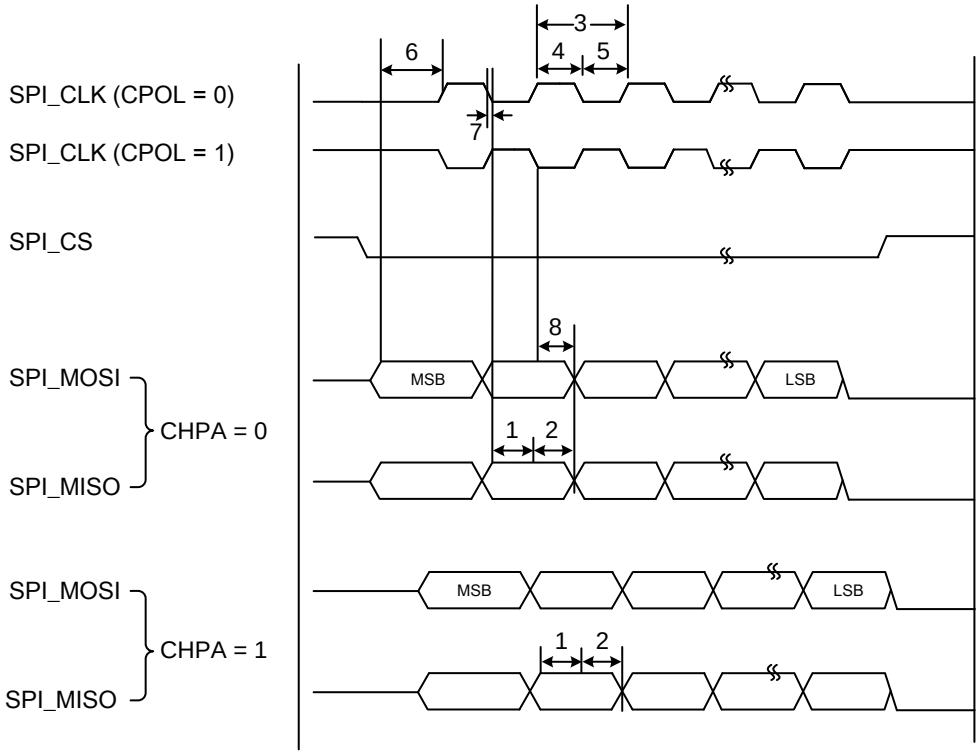


Figure 7–11 SPI Timings

7.4 Universal Asynchronous Receiver Transmitter (UART)

The SNC7352x series UART controller uses serial communication for data transmission. The UART offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. The UART of the SNC7352x series includes a programmable baud rate generator capable of dividing the module's reference clock by divisors to generate the correct UART baud rate.

Features of the UART controller include:

- Baud rates of up to 921600 bps
- One start bit, 8-bit data, and one or two stop bit format
- 16 bytes TX and 16 bytes RX FIFO buffer
- Register locations conform to 16650 industry standard
- Receiver FIFO trigger points at 1, 4, 8, and 14 bytes
- Built-in baud rate generator
- Software or hardware flow control

Table 7–6 Timing Requirements for UART Receiver

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	$t_{w(URXDB)}$	Pulse duration, receive data bit	0.96U[22]	1.05U[22]	ns
2	$t_{w(URXSB)}$	Pulse duration, receive start bit	0.96U[22]	1.05U[22]	

The table below lists switching characteristics over recommended operating conditions for the UART transmitter.

Table 7–7 Switching Characteristics for UART Transmitter

No.	Parameter		Device		Unit
			MIN.	MAX.	
3	$t_{w(URXDB)}$	Pulse duration, transmit data bit	U[22] - 2	U[22] + 2	ns
4	$t_{w(URXSB)}$	Pulse duration, transmit start bit	U[22] - 2	U[22] + 2	
5	$f_{(baud)}$	UART1 maximum programmable baud rate1	110	921600	bps
		UART2 maximum programmable baud rate	110	921600	

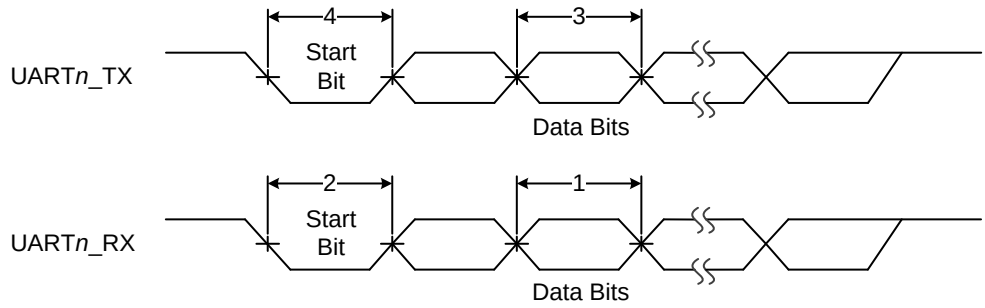


Figure 7–12 UART Transmit/Receive Timing

The SNC7352x series UART includes TX and RX pins for transmitting, receiving, and flow control. It has one start bit, 8-bit data, and one/two stop bits for each communication.

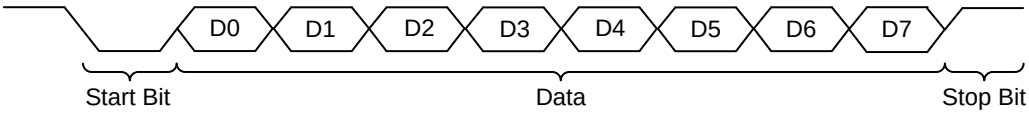


Figure 7–13 UART Transfer Format

7.5 32-bit Timer/Counter (CT32B)

The SNC7352x series provides eight 32-bit timers/counters. Each timer is designed to count cycles of the peripheral clock (PCLK) or an external clock. The timers/counters can optionally generate interrupts or perform other actions at specified timer values based on four match registers. Each timer has one capture input to trap the timer value during input signal transitions, optionally generating an interrupt.

[22] U = UART baud time = 1 / programmed baud rate.

Features of the timers/counters include:

- Eight 32-bit timers/counters
- Each with a programmable 32-bit pre-scale counter that controls division of PCLK before applying to the timer/counter.
- Four match registers for each timer/counter
- Generate interrupt signal when the match register matches the timer/counter value.

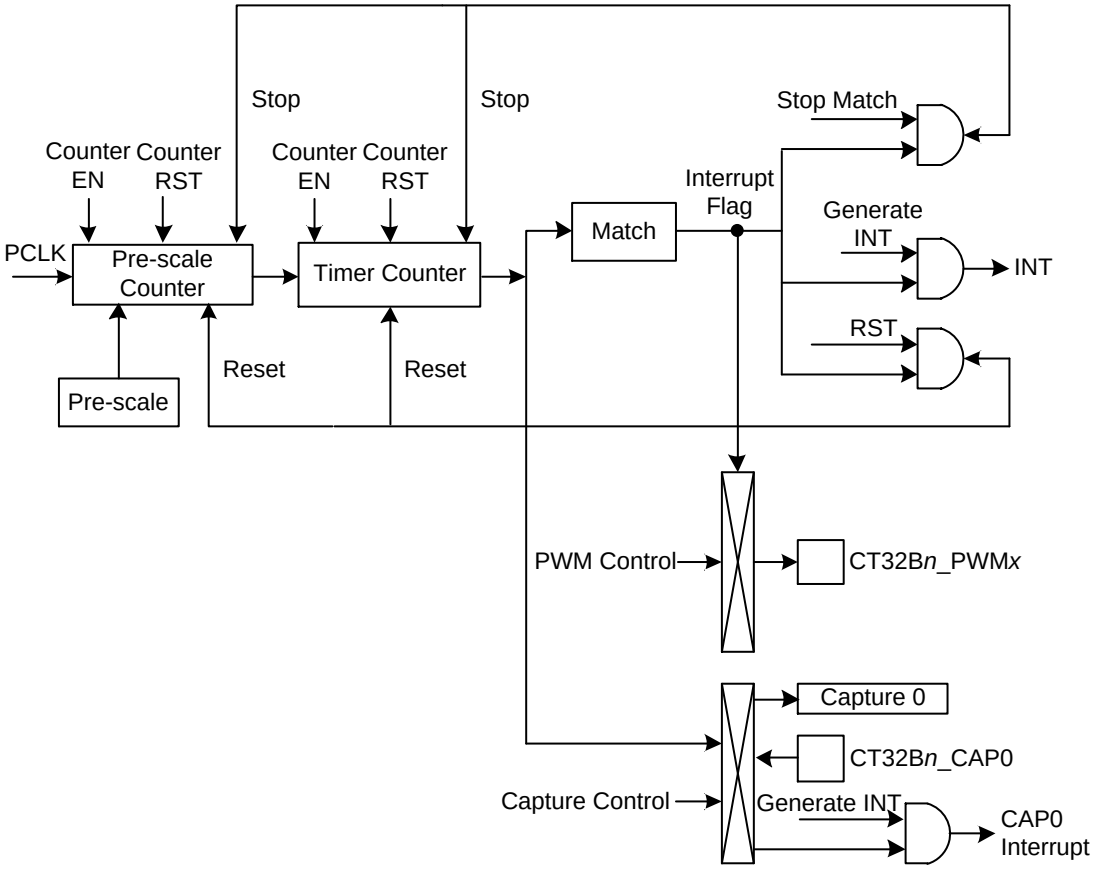


Figure 7–14 Timer/Counter Block Diagram

The capture function features frequency (time period) and pulse measurement. The capture registers are used to latch the value of the counter and timer after the CPU detects a transition applied at the CT32B*n*_CAP0 pin. CPU interrupt can be generated by setting the corresponding register flag. Features of the capture function include:

- Eight 32-bit capture channels that take a snapshot of the timer value during input signal transitions. Each capture event can generate an interrupt by option.
- Configurable timer and pre-scale counter that can be cleared on a designated capture event. This feature allows easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.

Configure the four modes of the capture function through the register.

- Timer mode: Capture on every rising edge.
- Counter mode: Capture on rising edges of the input signal.
- Counter mode: Capture on falling edges of the input signal.
- Counter mode: Capture on both edges of the input signal.

In PWM mode, up to three match registers can be used to provide a single-edge controlled PWM output on match output pins. Each match output can be independently set to perform either as PWM output or as match output controlled by the CT32B external match register.

7.6 Watchdog Timer (WDT)

The purpose of the WDT is to reset the MCU within a reasonable amount of time if it enters an erroneous state. When enabled, the WDT generates a system reset or interrupt if the user program fails to “feed” (or reload) the WDT within a predetermined amount of time. The WDT consists of a fixed pre-scaler that is divided by 128 and an 8-bit counter. The clock is fed to the timer via a pre-scaler. The timer decreases when clocked. The minimum value from the counter decrements is 0x01. Hence, the minimum WDT interval is *(TWDT_PCLK*[23] *× 128 × 1)* and the maximum WDT interval is *(TWDT_PCLK × 128 × 256)*. When the WDT is started by setting the register, the time constant value is loaded in the watchdog counter and the counter starts counting down. When the WDT is in the reset mode and the counter underflows, the CPU will be reset, loading the stack pointer and program counter from the vector table as in the case of external reset. Whenever the watchdog reset or interrupt is prevented by register setting, the WDT reset or interrupt occurs any time the watchdog is running and has an operating clock source.

Features of the WDT include:

- 8-bit watchdog counter
- Counter restart
- Generate reset signals
- Watchdog timer clock from 32 kHz SYS_ILRC
- Programmable assert duration of reset and interrupt
- Generate interrupts to the system

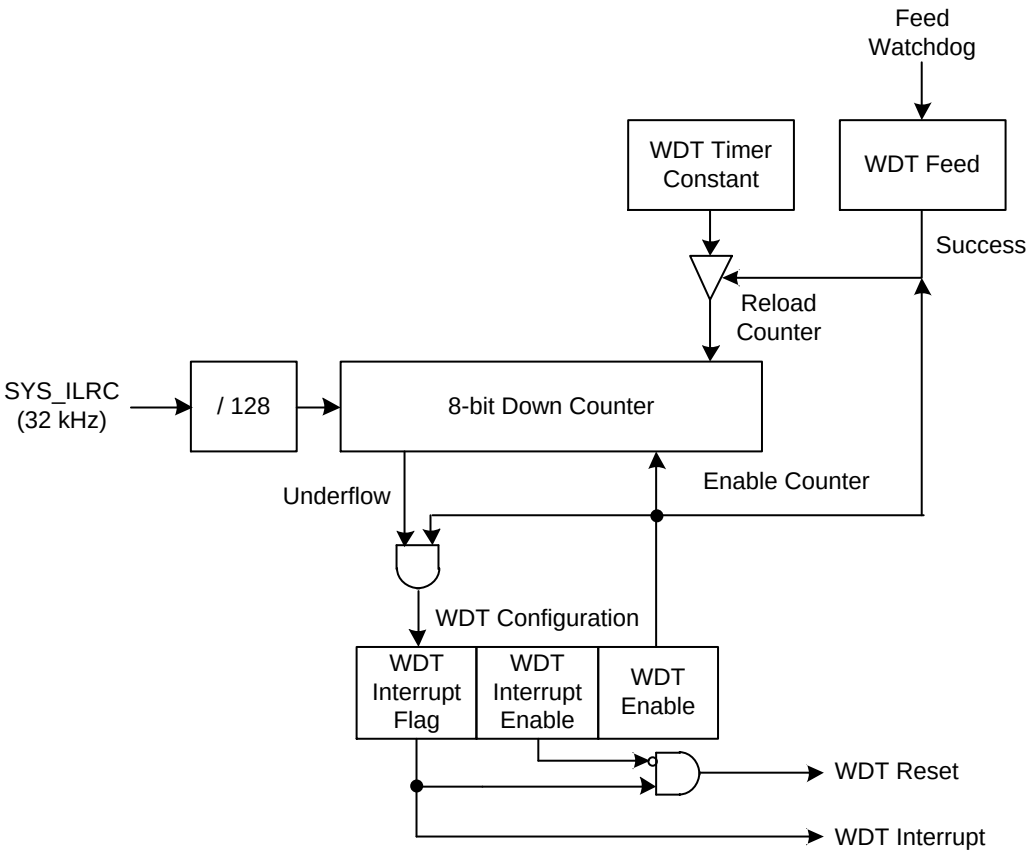


Figure 7–15 WDT Block Diagram

[23] PCLK = peripheral clock

7.7 Successive Approximation Register Analog-to-Digital Converter (SAR ADC)

The 10-bit SAR ADC converter has six input sources with up to 1024-step resolution to convert analog signals into 10-bits digital data. In the SNC7352x series provides an interrupt to indicate the ADC result is ready.

Features of the SAR ADC include:

- Input 0V to 3.3V full swing
- Conversion rate up to 1M SPS
- Low latency-time
- Supports 10-bit resource
- Supports 128/64/32/16/8/4/2/1 kHz audio conversion rate (system frequency = 162 MHz)
- Supports single mode and continuous mode

7.7.1 Timing

Table 7–8 Switching Characteristics for SAR ADC

No.	Parameter		Device		Unit
			MIN.	MAX.	
Digital Interface					
1	t_p	ADC clock period	61.7	–	ns
2	t_{HOLD}	ADC data hold time	956.79	–	μs
3	t_S	Sampling period	925.926	–	
–	F_S	Conversion rate	–	1.08	
Internal Clock					
4	t_1[24]	ADC setup time per conversion	246.8		ns
5	t_2[25]	ADC sampling time per conversion	185.1		
6	t_3[26]	ADC OS time per conversion	61.7		

[24] $t_1 = 4\ Tp$
[25] $t_2 = 3\ Tp$
[26] $t_3 = Tp$

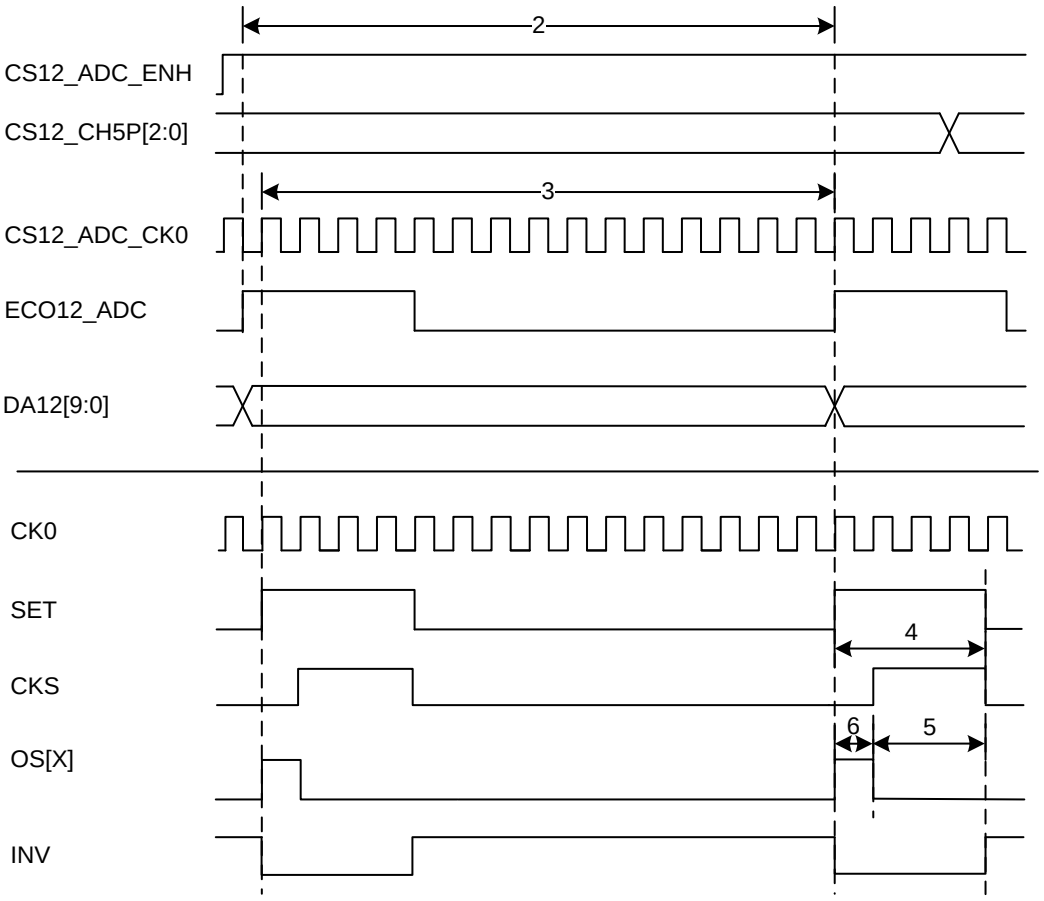


Figure 7–16 SAR ADC Timing

The figures below illustrate SAR ADC timings in single and continuous modes respectively. In continuous mode, the start bit is set before the conversion of the first sample data. When the first sample data conversion is completed, the hardware automatically sets the start bit for conversion of the next sample data to begin.

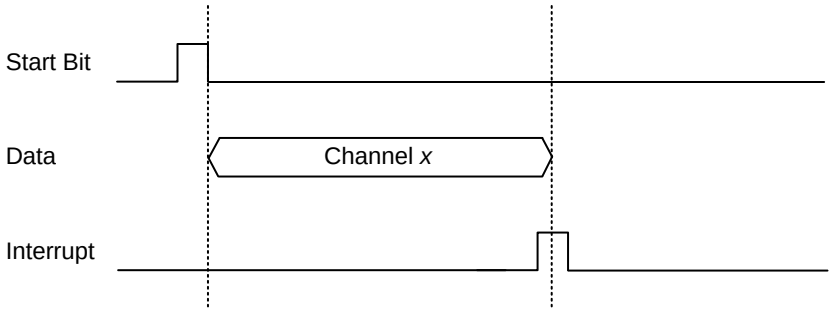


Figure 7–17 SAR ADC Single Mode Timing

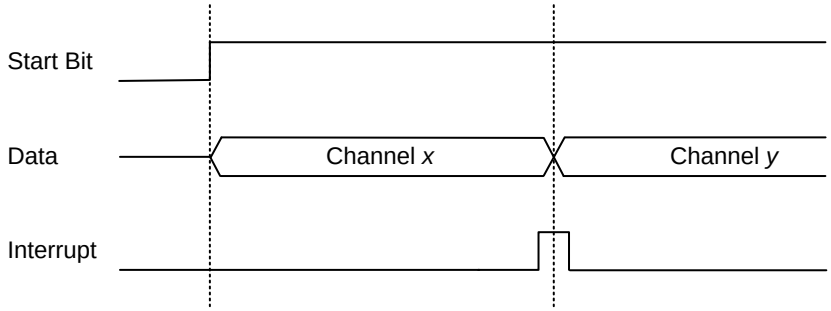


Figure 7–18 SAR ADC Continuous Mode Timing

7.8 SD/SDIO Controller (SD1)

Features of the SD/SDIO controller include:

- Built-in SD/SDIO controller
- Compliant with SD 2.0 specification
- Compliant with SDIO 2.0 specification
- Programmable clock frequency
- Auto multiple block read/write command
- DMA for large data transfers
- CRC-16 for the SD data
- Write-protect for the SD cards
- Card-detect for the SD cards

7.8.1 Timing

The table below lists timing requirements over the condition of SD clock = 162 / 2 / (*n* + 2) MHz, *n* = 0 for SD module.

Table 7–9 Timing Requirements for SD Module

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	$t_{su(CMDV–CLKH)}$	Setup time, SD_CMD valid before SD_CLK high	9	–	ns
2	$t_{h(CLKH–CMDV)}$	Hold time, SD_CMD valid after SD_CLK high	12	–	
3	$t_{SU(DATV–CLKH)}$	Setup time, SD_D[3:0] valid before SD_CLK high	6	–	
4	$t_{h(CLKH–DATV)}$	Hold time, SD_D[3:0] valid after SD_CLK high	7	–	

The table below lists switching characteristics over recommended operating conditions for SD module.

Table 7–10 Switching Characteristics for SD Module[27]

No.	Parameter		Device		Unit
			MIN.	MAX.	
5	$f_{(CLK)}$	Operating frequency	–	32[28]	MHz
6	$t_{W(CLKL)}$	Pulse width, SD_CLK low	0.5P[29]	–	ns
7	$t_{W(CLKH)}$	Pulse width, SD_CLK high	0.5P[29]	–	
8	$t_{r(CLK)}$	Rise time, SD_CLK	–	6	

[27] When initializing, the clock of the SD card should be less than 400 kHz.
[28] The SD clock delay is 1 idle clock (1/80 MHz) per byte transmission.
[29] P = SD_CLK period

No.	Parameter		Device		Unit
			MIN.	MAX.	
9	$t_{f(CLK)}$	Fall time, SD_CLK	–	6	ns
10	$t_{d(CLKL-CMD)}$	Delay time, SD_CLK low to SD_CMD transition	17	–	
11	$t_{d(CLKL-DAT)}$	Delay time, SD_CLK low to SD_D[3:0] transition	17	–	

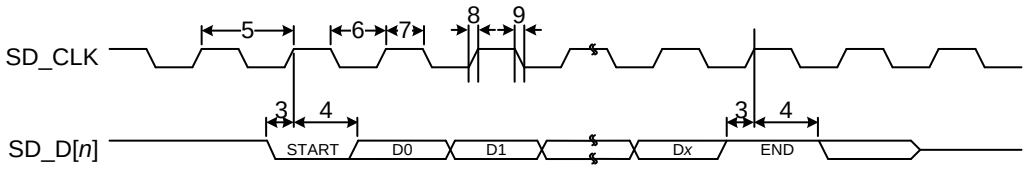


Figure 7–19 SD Host Read and Card CRC Status Timing

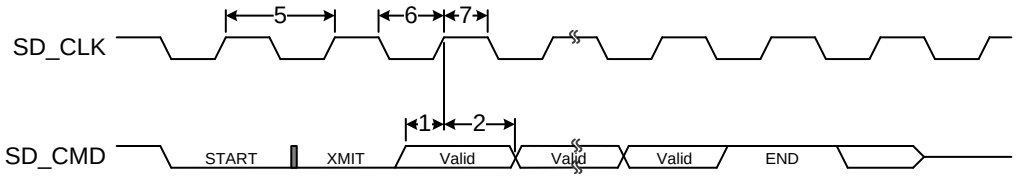


Figure 7–20 SD Card Response Timing

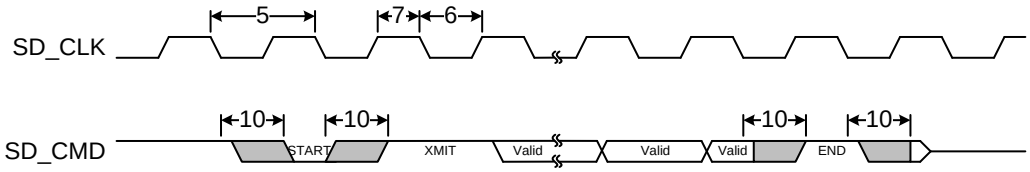


Figure 7–21 SD Host Command Timing

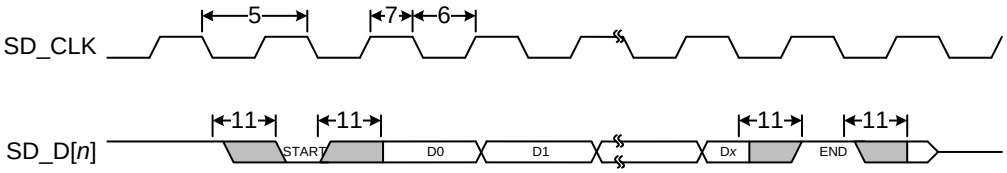


Figure 7–22 SD Host Write Timing

7.9 SPI Controller with DMA

The SNC7352x series has two SPI controllers with DMA to connect to a wide variety of SPI devices. The DMA data transmission avoids interruptions and increases CPU computing bandwidth. An ECC is built-in for the SPI NAND for error-bit detection and to correction.

Features of the SPI controller with DMA are:

- Master mode only
- 4 or 3-wire protocol
- 1-byte FIFO
- 1/2/4-bit TX/RX DMA mode
- 5, 10, 20, and 40 MHz clock frequencies
- Supports 1/4/8-bit ECC
- DMA access

7.9.1 Timing

Refer to 7.3 Serial Peripheral Interface (SPI). The hardware delays one idle clock (110 ns) in every 4 bytes.

7.10 Universal Serial Bus 2.0 (USB 2.0)

The SNC7352x series has one USB 2.0 controller with host/device option. The functions of the controller when being used as a host or a device are elaborated in subsections 7.10.1 and 7.10.2 respectively.

Features of the USB 2.0 host include:

- Two USB 2.0 hosts, each supporting an individual USB system
- USB 2.0 all transfer modes (control, bulk, isochronous, and interrupt)
- One port for root hub function
  - The companion host controller for full-speed (FS) and low-speed (LS) functionalities are fully supported, but it is not implemented based on the OHCI or UHCI standard.
- Port router is not required-Companion port route description for OHCI/UHCI
  - Bus topology
- Only high-speed (HS) hub plugged into tier one layer
- Device with HS control transfer/ HS bulk transfer/ HS isochronous transfer/ HS interrupt transfer/ FS control transfer/ FS bulk transfer/ FS interrupt transfer plugged into the root hub

The USB 2.0 host **does NOT** support

- FS ISO
- Transaction isochronous transfer descriptor (siTD)
- Frame span traversal node (FSTN)
- USB On-The-Go (OTG) and embedded host supplement

Features of the USB 2.0 device include:

- Compliant to USB 2.0 specification
- Compliant to AMBA 2.0 specification
- HS and FS supported
- Control transfer supported by endpoint #0
- One BULK-IN, one BULK-OUT, and one INT-IN endpoints
- Scatter-gather DMA
- 2.5k bytes (KB) FIFO RAM shared by all endpoints
- USB video class (UVC) bulk mode
- Mass storage class (MSC)
- Human interface device (HID)

The USB 2.0 device **does NOT** support isochronous transfer type.

7.10.1 USB 2.0 Host

The USB host function contains a universal serial bus (USB) 2.0 host controller and a built-in USB 2.0 host PHY. Without software intervention, the host controller can deal with a transaction-based data structure to offload the CPU and automatically transmit/receive data on the USB bus. The transceiver interface is UTMI+ level 3, which supports HS transfer with a HS hub. Without supporting siTD, FS with isochronous transfer device cannot be applied to USB 2.0 host via a HS hub or root hub.

I. AHB Interface

The EHCI host controller (HC) is connected to the system by the AHB. The design requires both master and slave bus operations. As a master, the host controller is responsible for running cycles on the AHB to access transfer descriptors as well as transferring data between memory and the local data buffer. As a slave, the host controller monitors the cycles on the AHB and determines when to respond to these cycles. Configuration and non-real-time control access to the host controller operational registers are through the AHB slave interface.

II. EHCI Controller

The EHCI supports two transfer types: asynchronous and periodic. The periodic transfer type includes isochronous and interrupt, and the asynchronous transfer type includes control and bulk.

III. Interrupt Processing

HC-initiated communication with the host controller driver by interrupts. There are several events that may trigger an interrupt from the host controller. Each specific event sets a specific bit in the interrupt status register.

IV. DMA

The DMA is the central block in the data path. The DMA coordinates all access to the AHB master interface. There are two sources of bus mastering within a host controller: the link list processor and the data buffer engine.

V. Data Buffer

The data buffer serves as the data interface between the AHB master and the USB protocol engine. It is a Ping-Pong FIFO RAM with 1024 bytes x 2 size.

VI. USB 1.1 Host Controller Interface

A new structure is created to substitute the OHCI/UHCI USB 1.1 control unit. The port routing logic was disregarded as there is only one port in root hub.

VII. Timing

Table 7–11 Switching Characteristics for USB 2.0 Host

Parameter		Device						Unit
		Low-Speed		Full-Speed		High-Speed		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{r(D)}$	Rise time, USB_DP and USB_DM signals[30]	75	300	4	20	0.5	20	ns
$t_{f(D)}$	Fall time, USB_DP and USB_DM signals[30]	75	300	4	20	0.5	20	
t_{frfm}	Rise/fall time, matching[31]	80	125	90	111.11	–	–	%

[30] Low Speed: CL = 200 pF, Full Speed: CL = 50 pF; High Speed: CL = 50 pF
[31] t_{frfm} = (t_r / t_f) x 100; excluding the first transaction from the idle state

Parameter		Device						Unit
		Low-Speed		Full-Speed		High-Speed		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{CRS}	Output signal cross-over voltage[30]	1.3	2	1.3	2	–	–	V
$t_{jr(source)NT}$	Source (host) driver jitter, next transition	–	2	–	2	–	–	ns
$t_{jr(FUNC)NT}$	Function driver jitter, next transition	–	25	–	2	–	–	
$t_{jr(source)PT}$	Source (host) driver jitter, paired transition[32]	–	1	–	1	–	–	
$t_{jr(FUNC)PT}$	Function driver jitter, paired transition	–	10	–	1	–	–	
$t_{w(EOPT)}$	Pulse duration, EOP transmitter	1250	1500	160	175	–	–	
$t_{w(EOPR)}$	Pulse duration, EOP receiver	670	–	82	–	–	–	
$t_{(DRATE)}$	Data rate	–	1.5	–	12	–	480	Mb/s
Z_{DRV}	Driver output resistance	–	–	28	49.5	40.5	49.5	Ω

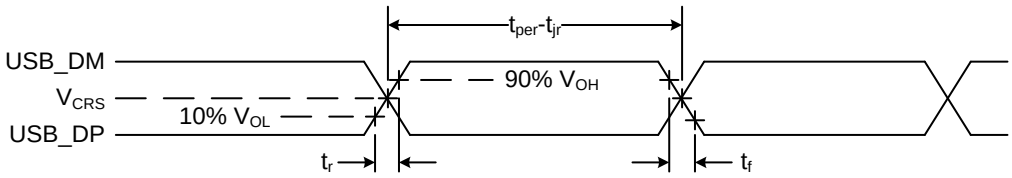


Figure 7–23 USB 2.0 Host Integrated Transceiver Interface Timing

7.10.2 USB 2.0 Device

Other than a USB host, the SNC7352x series has a USB 2.0 high speed device interface, forward compatible with full speed mode. That enables the SNC7352x series to be a USB device supporting bulk, isochronous, interrupt, and control transfers that are compliant to the USB 2.0 specification.

The USB controller transfers data through the AHB and the USB. The AHB includes the AHB master interface and AHB slave interface. The CPU programs the USB controller through the AHB slave interface. For IN or OUT transfer, the USB controller writes data to system memory or reads data from system memory through the AHB master interface. The USB controller also includes a USB transceiver as the interface of the USB.

USB endpoints: includes nine endpoints, designated EP0, EP1, EP3, EP4, EP5, EP7, EP12, EP13, EP14, and EP15. Each is intended for a particular use as below:

- EP0: the default endpoint uses control transfer (in/out) to handle configuration and control functions required by the USB specification.
- EP1: Interrupt in endpoint
- EP3: Isochronous in endpoint
- EP4: Isochronous out endpoint
- EP5: Interrupt in endpoint
- EP7: Isochronous in endpoint
- EP12: Bulk in endpoint
- EP13: Bulk out endpoint
- EP14: Bulk in endpoint
- EP15: Bulk out endpoint

[32] $t_{jr} = t_{px(1)} - t_{px(0)}$

I. Timing

Table 7–12 Switching Characteristics for USB 2.0 Device

Parameter		Full Speed		High Speed		Unit
		MIN.	MAX.	MIN.	MAX.	
$t_{r(D)}$	Rise time, USB_DP and USB_DM signals[30]	4	20	0.5	20	ns
$t_{f(D)}$	Fall time, USB_DP and USB_DM signals[30]	4	20	0.5	20	
t_{rfm}	Rise/fall time, matching[31]	90	111.11	–	–	%
V_{CRS}	Output signal cross-over voltage[30]	1.3	2	–	–	V
$t_{jr(source)NT}$	Source (host) driver jitter, next transition	–	2	–	–	ns
$t_{jr(FUNC)NT}$	Function driver jitter, next transition	–	2	–	–	
$t_{jr(source)PT}$	Source (host) driver jitter, paired transition[32]	–	1	–	–	
$t_{jr(FUNC)PT}$	Function driver jitter, paired transition	–	1	–	–	
$t_{w(EOPT)}$	Pulse duration, EOP transmitter	160	175	–	–	
$t_{w(EOPR)}$	Pulse duration, EOP receiver	82	–	–	–	
$t_{(DRATE)}$	Data rate	–	12	–	480	Mb/s
Z_{DRV}	Driver output resistance	28	49.5	40.5	49.5	Ω

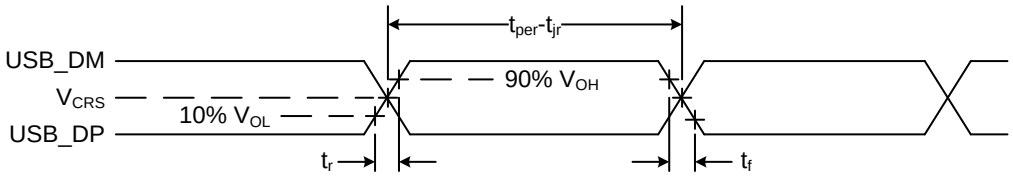


Figure 7–24 USB 2.0 Device Integrated Transceiver Interface Timing

8 Multimedia

8.1 CMOS Image Sensor (CIS) Interface

The CIS interface is an advanced 12-pin interface consisting of a CIS clock, VSYNC, HREF, pixel clock and eight data lines. The frequency of the CIS clock which outputs to the CIS module can be configured as MCLK / 2, MCLK / 4 or MCLK / 8. VSYNC, HSYNC and the pixel clock signals from the CIS module can be configured for active timing as rising or falling edge. An interrupt flag will be issued after a line of data is transmitted to RAM, which informs the system to access data that is stored at Window Random Access Memory (WRAM).

Features of the CIS interface are:

- Supports image resolution in VGA (640 x 480), CIF (352 x 288), QVGA (320 x 240), QCIF (176 x 144), and QQVGA (160 x 120)
- Supports image data formats in YUV422 and 8-bit RGB
- Adjustable VSYNC, HREF and pixel clock edge trigger selection
- Adjustable clock output, system clock divided by 2, 4, or 8
- Output image cropping and scaling
- Supports Line to block (L2B) mode for CSC and JPEG encoder
- Supports three line buffers, Line 0, Line 1, and Line 2[33]
- RGB and YUV data mode to DRAM or SRAM by DMA, but L2B mode to DRAM is not available.

WARNING The system crushes when using cropping and scaling functions at the same time.

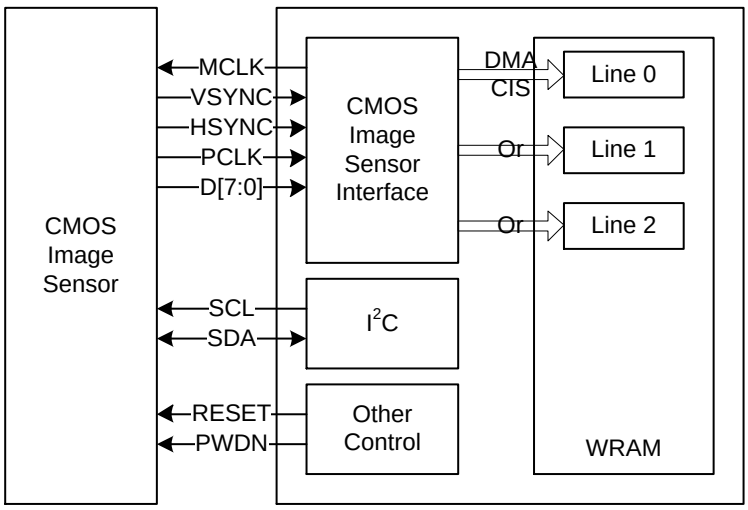


Figure 8–1 CIS Interface Block Diagram

[33] When L2B mode is enabled, set the size of the line buffer = frame width x 8.

8.1.1 Timing

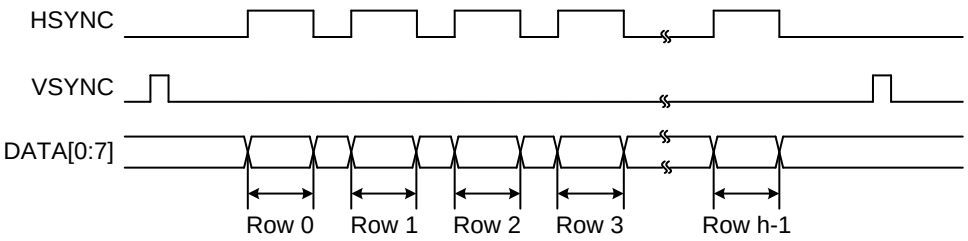


Figure 8–2 CIS Interface Timing

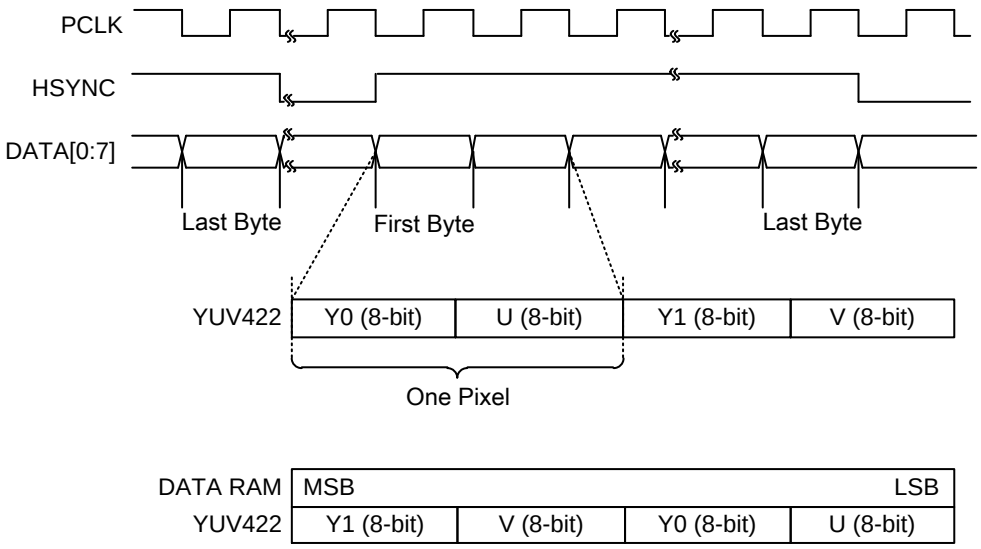


Figure 8–3 CIS Data Format

8.2 Color Space Converter (CSC)

The CSC converts pixel data from YCbCr422 or 420 to RGB565 format. Features of the CSC are:

- Direct raw data to line buffer movement
- RGB output sequence: R0, G0, B0; R1, G1, B1
- YCbCr422 input sequence:
  Y1, Y0; Y3, Y2; Cb23, Cb01; Cr23, Cr01
  Y5, Y4; Y7, Y6; Cb67, Cb34; Cr67, Cr34
- YCbCr420 input sequence:
  Y1, Y0; Y3, Y2; Cb4567, Cb0123; Cb4567, Cr0123
  Y5, Y4; Y7, Y6; Cb4567, Cb0123; Cr4567, Cb0123
- Dithering and scaling mode
  Supports nine-tap FIR filters to avoid aliasing and false color when scaling down. The value should be:

Filter0 + (Filter1 + Filter2 + Filter3 + Filter4) x 2 = 256

8.3 JPEG Codec

The JPEG codec of the SNC7352x series supports JFIF format and functions either in encoder or decoder mode at the same time.

Features of the JPEG codec are:

- Video rate JPEG encode and decode
- Baseline DCT, fixed quantization table (two AC and two DC typical Huffman tables at ISO/IEC10918-1)
- Supports scaling quantization table ranging from 000.00001(B)–111.11111(B)
- JPEG File Interchange Format (JFIF)
- Format: YCbCr422 and 420 (depending on the external block function)
- Sharing DCT, zig-zag, quantizer and FIFO for encoder and decoder
- Encoder format:
  Block input: YCbCr422: 16 x 8 pixels; YCbCr420: 16 x 16 pixels, 8-bit data input
  Output: JPEG bit-stream, 8-bit data output
- Decoder format:
  Input: JPEG bit-stream in 8-bit data input
  Block output: YCbCr422: 16 x 8 pixels; YCbCr420: 16 x 16 pixels, 8-bit data output

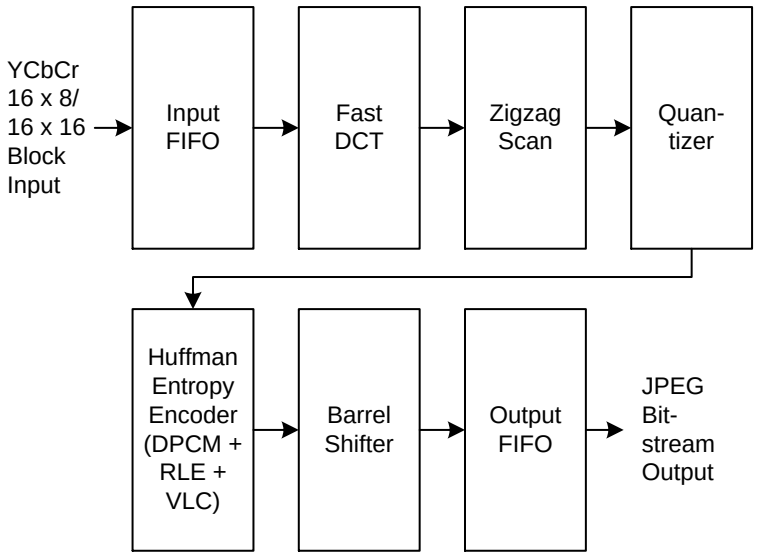


Figure 8–4 Encoder Hardware Block Diagram

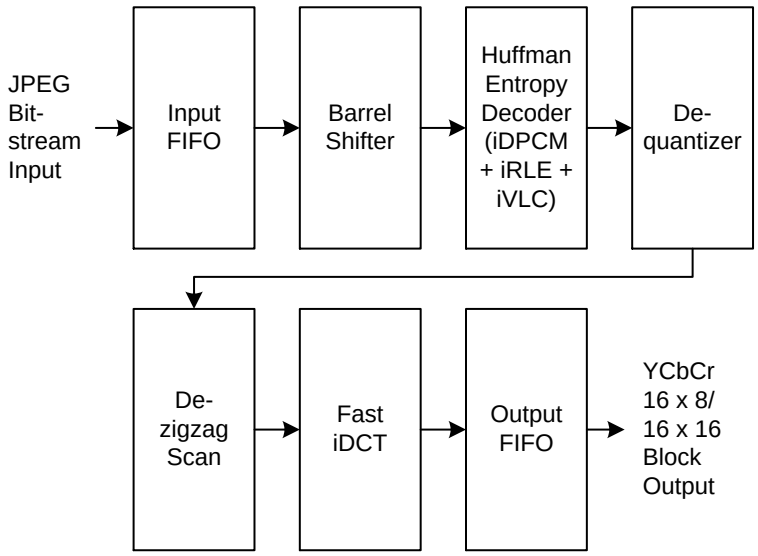


Figure 8–5 Decoder Hardware Block Diagram

8.4 TFT-LCD Interface

The built-in TFT-LCD interface supports serial and parallel RGB modes (UPS051/UPS052) in RGB565 format with a resolution of up to 480 x 272.

8.4.1 Timing

Table 8–1 Switching Characteristics for TFT-LCD

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	t_H	Horizontal line	0	4 x (2^{15} - 1)	DCLK[34]
2	t_{hsw}	Horizontal sync pulse width	0	2^{15} - 1	
3	t_{hblk}	Horizontal sync blanking	0	2 x (2^{15} - 1)	
4	t_{hdisp}	Horizontal display area	0	2^{15} - 1	
5	t_{hfp}	Horizontal sync front porch	0	2^{15} - 1	
6	t_V	Vertical sync period time	0	4 x (2^{15} - 1)	t_H
7	t_{vsw}	Vertical sync pulse width	0	2^{15} - 1	
8	t_{vblk}	Vertical sync blanking	0	2 x (2^{15} - 1)	
9	t_{vdisp}	Vertical display area	0	2^{15} - 1	
10	t_{vfp}	Vertical sync front porch	0	2^{15} - 1	

[34] DCLK = 162 MHz / (CLK_PreScaler + 1); CLK_PreScaler = 0–65535

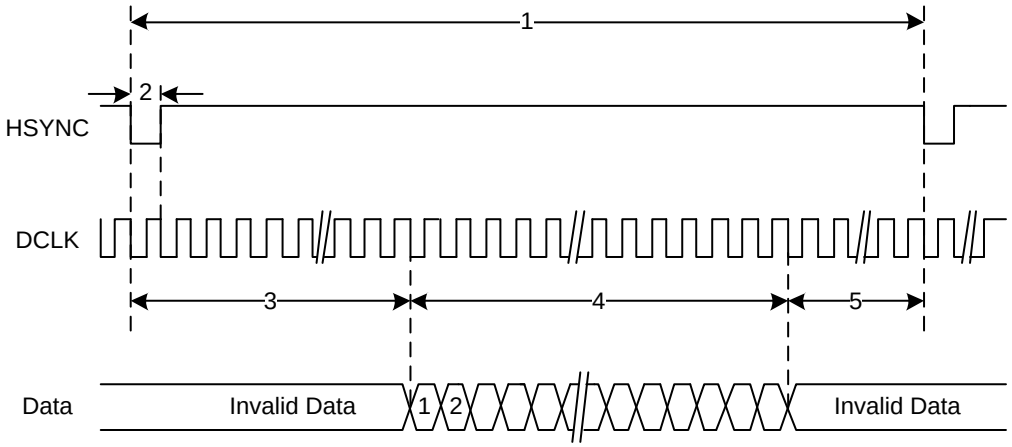


Figure 8–6 TFT-LCD Horizontal Timing

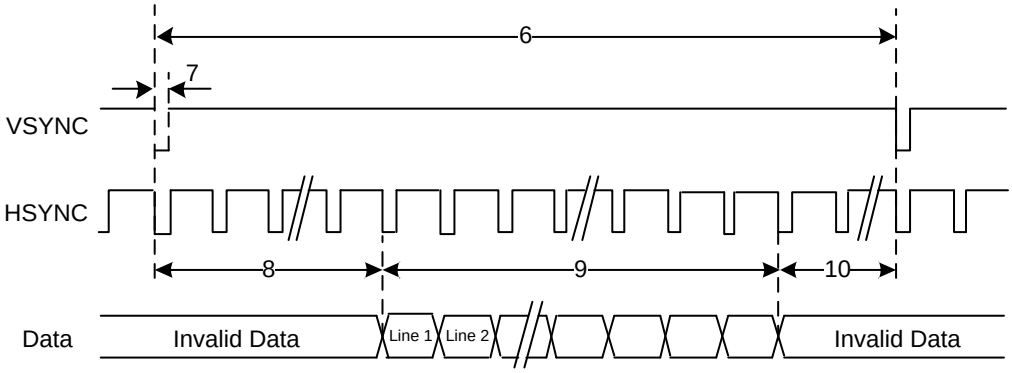


Figure 8–7 TFT-LCD Vertical Timing

8.5 8080 MCU Interface

The 8080 MCU interface for communication between the MCU controller and a LCD driver chip includes 8 or 16 bi-directional data lines, one chip-select line (CS), one writing-latch line (WR)/one reading-latch line (RD), and one data/command select line (A0).

Features of the 8080 MCU interface are:

- 8/16-bit data space
- Auto access word data for the lower 8-bit data bus (high byte first or low byte first)
- Adjustable access signal pulse

8.5.1 Timing

The clock delay of 8080 MCU interface is 1 idle clock (1 / 162 MHz) per 16-bit transmission.

Table 8–2 Switching Characteristics for 8080 MCU Interface

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	t_{PWLW}	Write low time	1 / 162 MHz x (0 + 1)	1 / 162 MHz x (255 + 1)	ns
2	t_{PWHW}	Write high time	1 / 162 MHz x (0 + 1)	1 / 162 MHz x (255 + 1)	
3	t_F	Fall time	6		
4	t_R	Rise time	6		

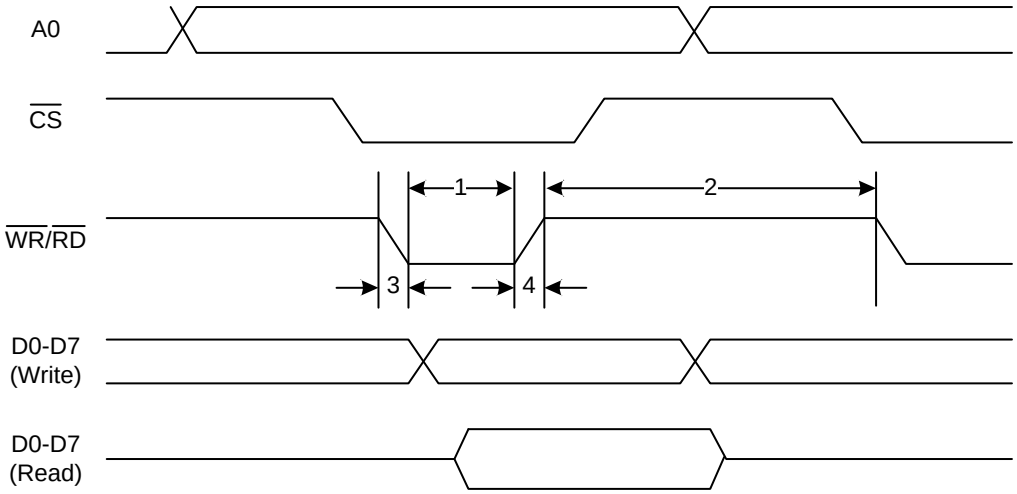


Figure 8–8 8080 MCU Interface Timings

8.6 Audio-I²S

The audio system of the SNC7352x series has five sets of I²S. I²S0 to I²S3 support slave mode with DMA and connect to multiple audio codecs such as SNAUD01. I²S4 supports slave and mater mode and is dedicated to communicate with other master chips.

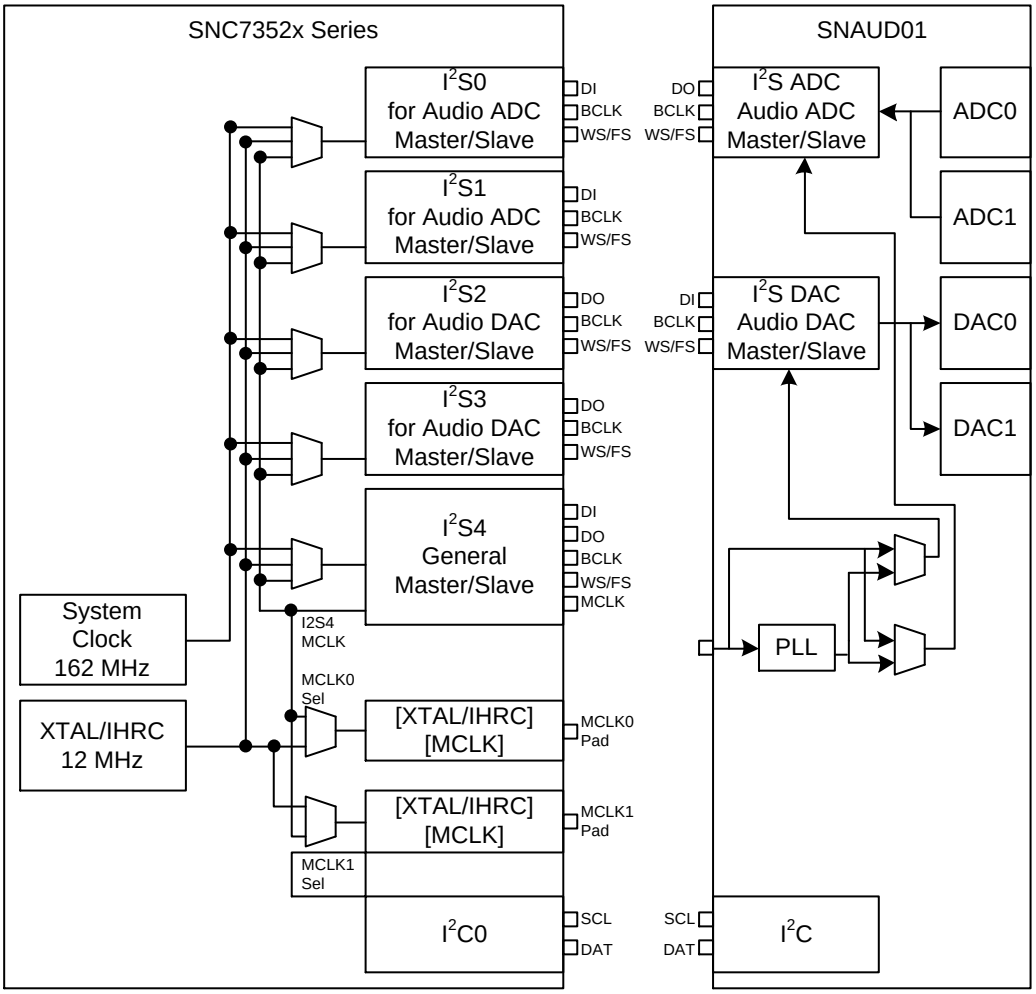


Figure 8–9 Audio Block Diagram

Features of the I²S include:

- Master or slave mode
- 8/16/24/32-bit data length
- Mono and stereo audio data
- I²S and MSB justified data format
- Provides 8-word (32-bit) FIFO data buffers
- Generate interrupt requests when buffer levels cross a programmable boundary
- Independent reset, stop, and mute control options for I²S input and output

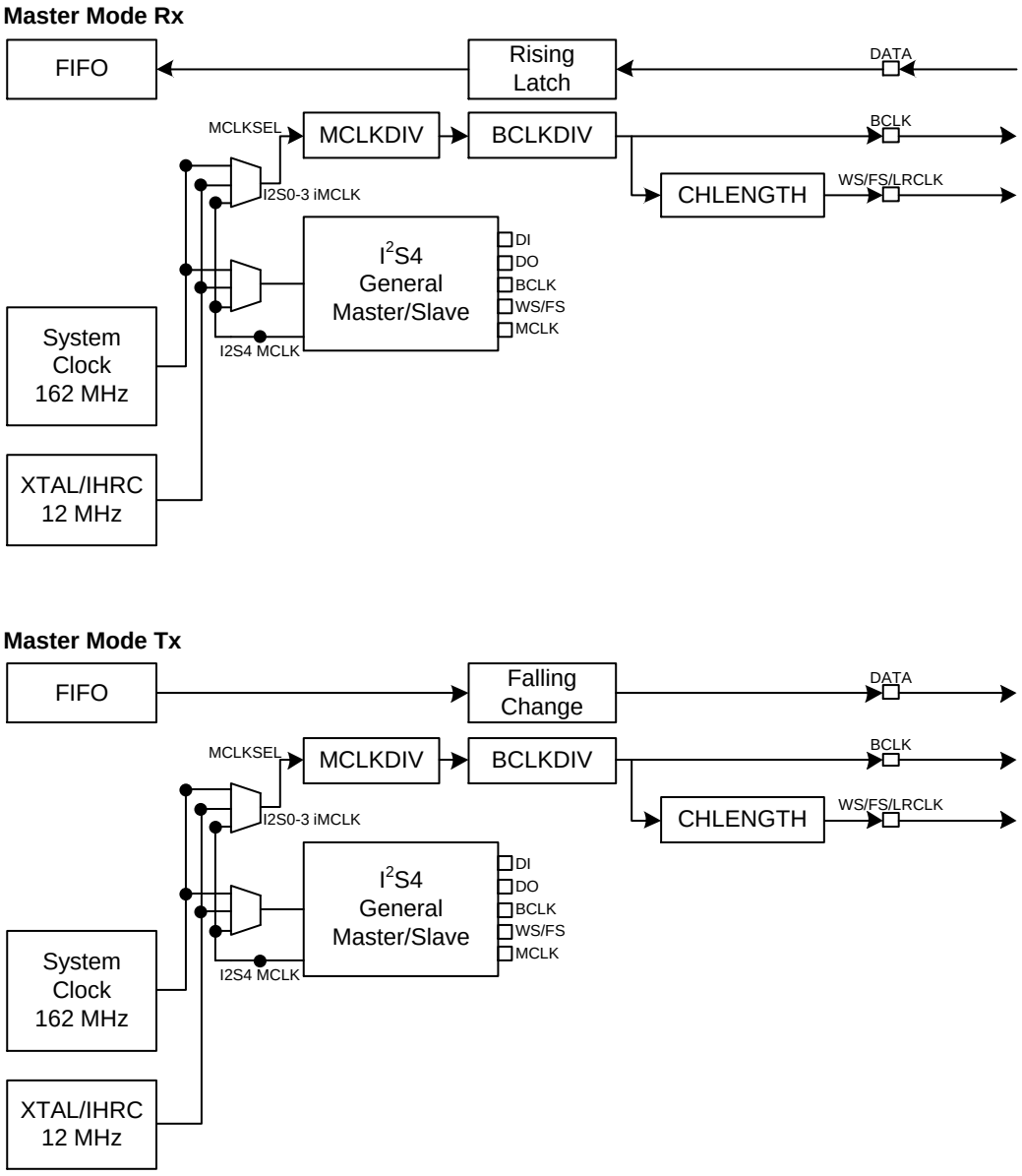


Figure 8–10 I²S Master Mode Block Diagram

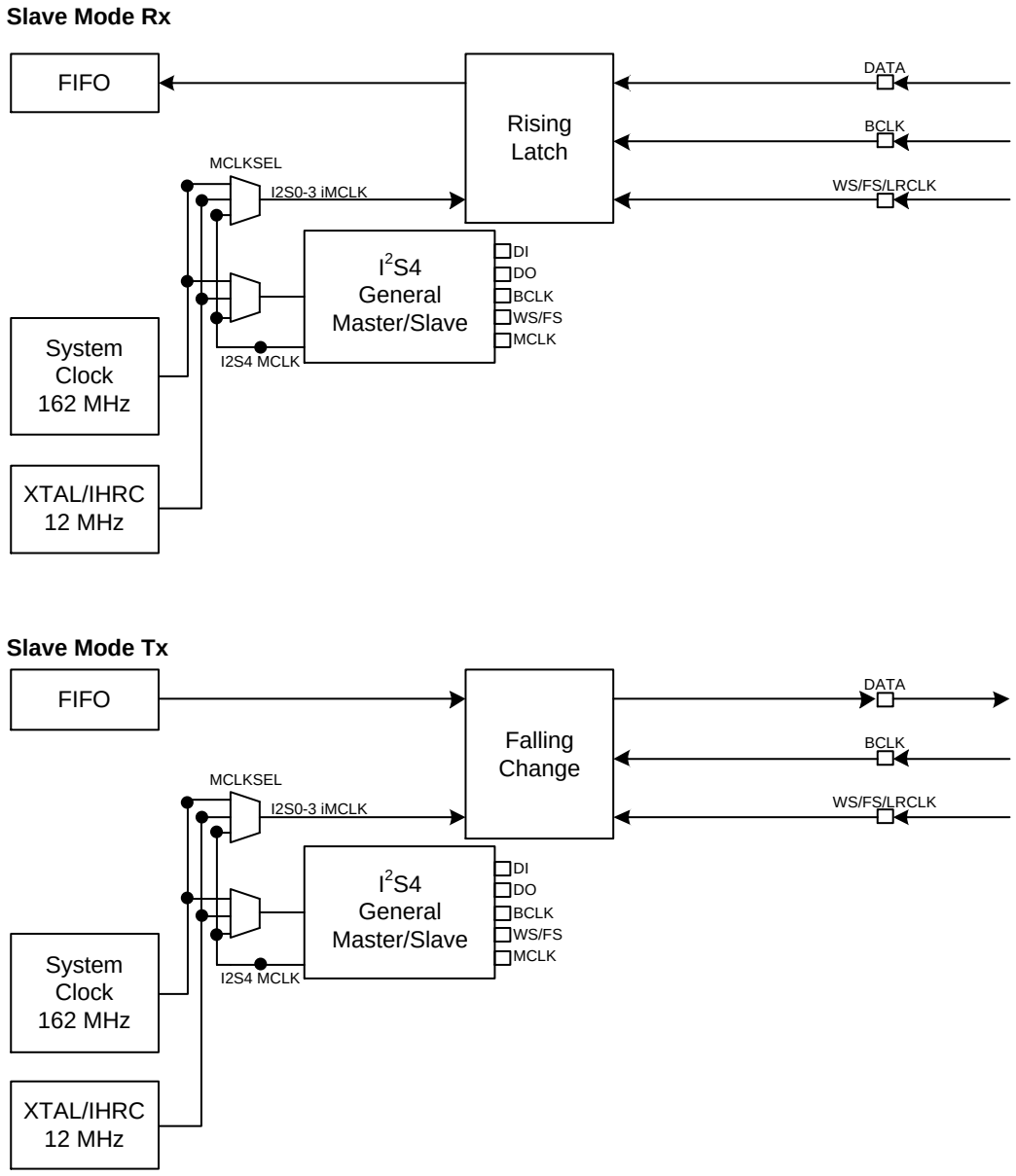


Figure 8–11 I²S Slave Mode Block Diagram

8.6.1 Timing

Table 8–3 Input Timing Requirements for I²S Master Receiver

Parameter		Device		Unit
		MIN.	MAX.	
$t_{su(SDR-BCK)}$	Setup time, I2S_DATA_IN valid before I2S_BCLK rising edge	0.2 ($t_{c(BCK)}$)	–	ns
$t_{h(BCK-SDR)}$	Output hold time, I2S_DATA_OUT valid after receive rising edge of I2S_BCLK	2	–	

Table 8–4 Input Timing Requirements for I²S Slave Receiver

Parameter		Device		Unit
		MIN.	MAX.	
$t_{c(BCK)}$	Cycle time, I2S_BCLK	80	10200	ns
$t_{w(BCKH)}$	Pulse width, I2S_BCLK high	0.35 ($t_{c(BCK)}$)	–	
$t_{w(BCKL)}$	Pulse width, I2S_BCLK low	0.35 ($t_{c(BCK)}$)	–	
$t_{su(SDR-BCK)}$	Setup time, I2S_DATA_IN valid before receive rising edge of I2S_BCLK	0.2 ($t_{c(BCK)}$)	–	
$t_{h(BCK-SDR)}$	Output hold time, I2S_DATA_OUT valid after receive rising edge of I2S_BCLK	2	–	

Table 8–5 Input Timing Requirements for I²S Slave Transmitter

Parameter		Device		Unit
		MIN.	MAX.	
$t_{c(BCK)}$	Cycle time, I2S_BCLK	80	10200	ns
$t_{w(BCKH)}$	Pulse width, I2S_BCLK high	0.35 ($t_{c(BCK)}$)	–	
$t_{w(BCKL)}$	Pulse width, I2S_BCLK low	0.35 ($t_{c(BCK)}$)	–	
$t_{r(BCK)}$	Rise time, I2S_BCLK	–	0.15 ($t_{c(BCK)}$)	

Table 8–6 Switching Characteristics for I²S Master Receiver

Parameter		Device		Unit
		MIN.	MAX.	
$t_{c(BCK)}$	Cycle time, I2S_BCLK	200[35]	10200	ns
$t_{w(BCKH)}$	Pulse width, I2S_BCLK high	0.4 ($t_{c(BCK)}$)	–	
$t_{w(BCKL)}$	Pulse width, I2S_BCLK low	0.4 ($t_{c(BCK)}$)	–	

Table 8–7 Switching Characteristics for I²S Master Transmitter

Parameter		Device		Unit
		MIN.	MAX.	
$t_{c(BCK)}$	Cycle time, I2S_BCLK	200[35]	10200	ns
$t_{w(BCKH)}$	Pulse width, I2S_BCLK high	0.4 ($t_{c(BCK)}$)	–	
$t_{w(BCKL)}$	Pulse width, I2S_BCLK low	0.4 ($t_{c(BCK)}$)	–	
$t_{d(BCK-LRCK\_SDX)}$	Delay time, I2S_BCLK rising edge to I2S_DATA_OUT output	–	0.5 ($t_{c(BCK)}$) + 5	
$t_{h(BCK-LRCK\_SDX)}$	Output hold time, I2S_DATA_OUT valid after receive rising edge of I2S_BCLK	0.5 ($t_{c(BCK)}$) - 5	–	
$t_{r(BCK)}$	Rise time, I2S_BCLK	–	20	

Table 8–8 Switching Characteristics for I²S Slave Transmitter

Parameter		Device		Unit
		MIN.	MAX.	
$t_{d(BCK-LRCK\_SDX)}$	Delay time, I2S_BCLK rising edge to I2S_DATA_OUT output	–	0.5 ($t_{c(BCK)}$) + 15	ns
$t_{h(BCK-LRCK\_SDX)}$	Output hold time, I2S_DATA_OUT valid after receive rising edge of I2S_BCLK	0.35 ($t_{c(BCK)}$)	–	

[35] The minimum period of the master clock is 40 ns and the minimum period of BCK is two master clock cycles. But considering the period of BCK is three master clock cycles, the minimum pulse width (high or low) of BCK is 0.33 ($t_{c(BCK)}$) which violates the I²S input timing requirement. To meet the input timing requirement, the minimum period of BCK is five master clock cycles.

The I²S is a standard interface for general use. Since the audio controller supports mono and stereo, the data is valid in first 8/16/24/32-bit from MSB in left channel of its timing diagram.

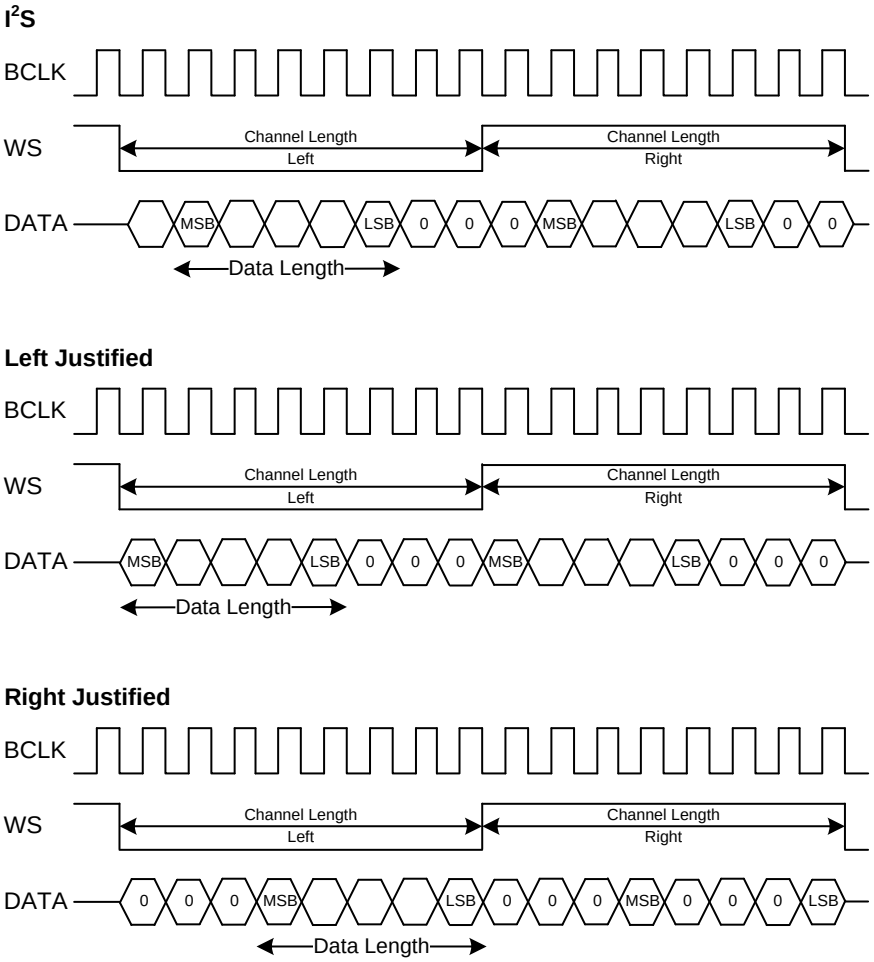


Figure 8–12 I²S Timings when Channel Length > Data Length

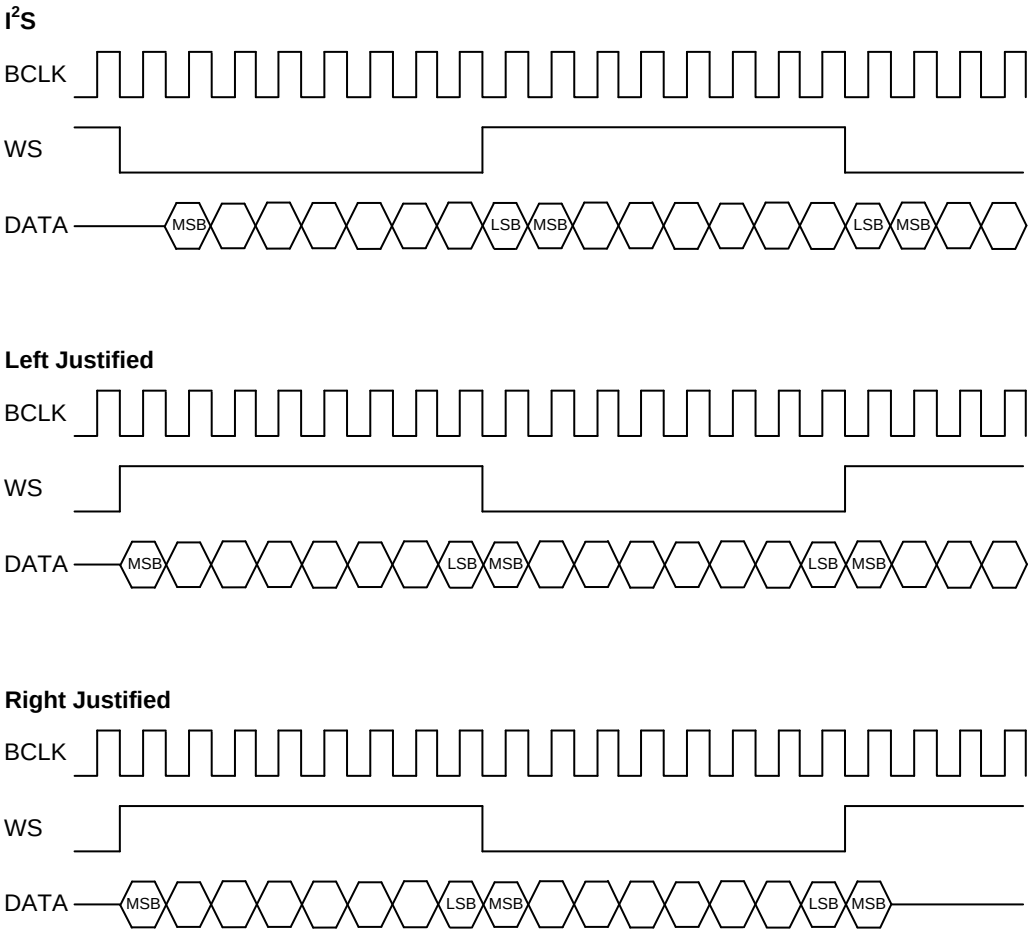


Figure 8–13 I²S Timings when Channel Length = Data Length

9 Device Operating Conditions

9.1 Absolute Maximum Ratings

Table 9–1 Absolute Maximum Ratings[36] [37]

Parameter		MIN.	MAX.	Unit
Supply voltage	V_{DD12}	-0.3	1.28	V
	V_{DD18_DRAM}	-0.3	1.90	
	V_{DD33}	-0.3	3.63	
Input voltage	V_{IN} (1.2V)	-0.3	1.28	
	V_{IN} (1.8V)	-0.3	1.90	
	V_{IN} (3.3V)	-0.3	3.63	
Ambient temperature	T_A	0	85	°C
Junction temperature	T_J	-40	125	
Storage temperature	T_{STG}	-40	125	

9.2 Recommended Operating Conditions

Table 9–2 Recommended Operating Conditions

Parameter	MIN.	TYP.	MAX.	Unit
Device supply voltage, I/O, V_{DD33}	2.93	3.30	3.63	V
Device supply voltage, V_{DD18_DRAM}	1.75	1.82	1.90	
Device supply voltage, V_{DD12} (normal mode)	1.17	1.22	1.28	
Device supply voltage, V_{DD12} (suspend mode)	0.95	0.99	1.04	
Supply ground, V_{SS}	0			
Ambient temperature, T_A	0	–	85	°C
Junction temperature, T_J	-40	–	125	

[36] Long-term exposure to absolute maximum ratings may affect device reliability, and permanent damage may occur if the operation exceeds the maximum ratings.
[37] All voltage values are with respect to VSS.

9.3 Electrical Characteristics

Table 9–3 Electrical Characteristics over Recommended Ranges

Parameter		Conditions (T_A = 25 °C)	MIN.	TYP.	MAX.	Unit
Normal current 40.5 MHz	$I_{NOR40.5}$	Dual core program run; no I/O toggle	–	20	–	mA
Normal current 81 MHz	I_{NOR81}	Dual core program run; no I/O toggle	–	30	–	
Normal current 162 MHz	I_{NOR162}	Dual core program run; no I/O toggle	–	50	–	
Deep power-down current	I_{DPD}	VDD = 3.3V; internal LDO 1.1/1.8V off, all clocks off	–	4	8	µA
Deep sleep current	I_{DSLP}	All clocks off	–	2.3	12	mA
IHRC	F_{IHRC}	Accuracy to ±2.0%	11.76	12	12.24	MHz
ILRC	F_{ILRC}	For WDT frequency	–	32	–	kHz
SAR ADC ENOB	ENOB	–	–	9	–	bit(s)
SAR ADC DNL	DNL	–	-2	–	2	LSB
SAR ADC INL	INL	–	-2	–	2	
Internal pull-up/pull-down resistance	R_{PU}/R_{PD}	–	30k	40k	66k	Ω
Internal pull-down resistance	R_{PD}	–	30k	40k	66k	
IO driving CFG0[38]	IO_{CFG0}	All GPIOs except SAR I/O	2	4.2	6	mA
IO driving CFG1[38] (default)	IO_{CFG1}		4	8.2	12	
IO driving CFG2[38]	IO_{CFG2}		6	12.2	18	
IO driving CFG3[38]	IO_{CFG3}		8	15.7	24	
IO sink CFG0[38]	IO_{CFG0}		2	3.8	6	
IO sink CFG1[38] (default)	IO_{CFG1}		4	7.4	12	
IO sink CFG2[38]	IO_{CFG2}		6	11	18	
IO sink CFG3[38]	IO_{CFG3}		8	14.3	24	
SAR I/O driving CFG0	AIO_{CFG0}	P0.4–P0.7/P4.2–P4.3	5	10	17	
SAR I/O driving CFG1 (default)	AIO_{CFG1}		10	21.8	35	
SAR I/O driving CFG2	AIO_{CFG2}		15	25.2	51	
SAR I/O driving CFG3	AIO_{CFG3}		20	27.4	68	
SAR I/O sink CFG0	AIO_{CFG0}		5	10	17	
SAR I/O sink CFG1 (default)	AIO_{CFG1}		10	21.0	35	
SAR I/O sink CFG2	AIO_{CFG2}		15	23.9	51	
SAR I/O sink CFG3	AIO_{CFG3}		20	26.5	68	

[38] CFG*x* represents the configurations of GPIO Port *n* driving control register (*x* = 0–3; *n* = 0–4).

9.4 Power Sequence

9.4.1 Power-up Sequence

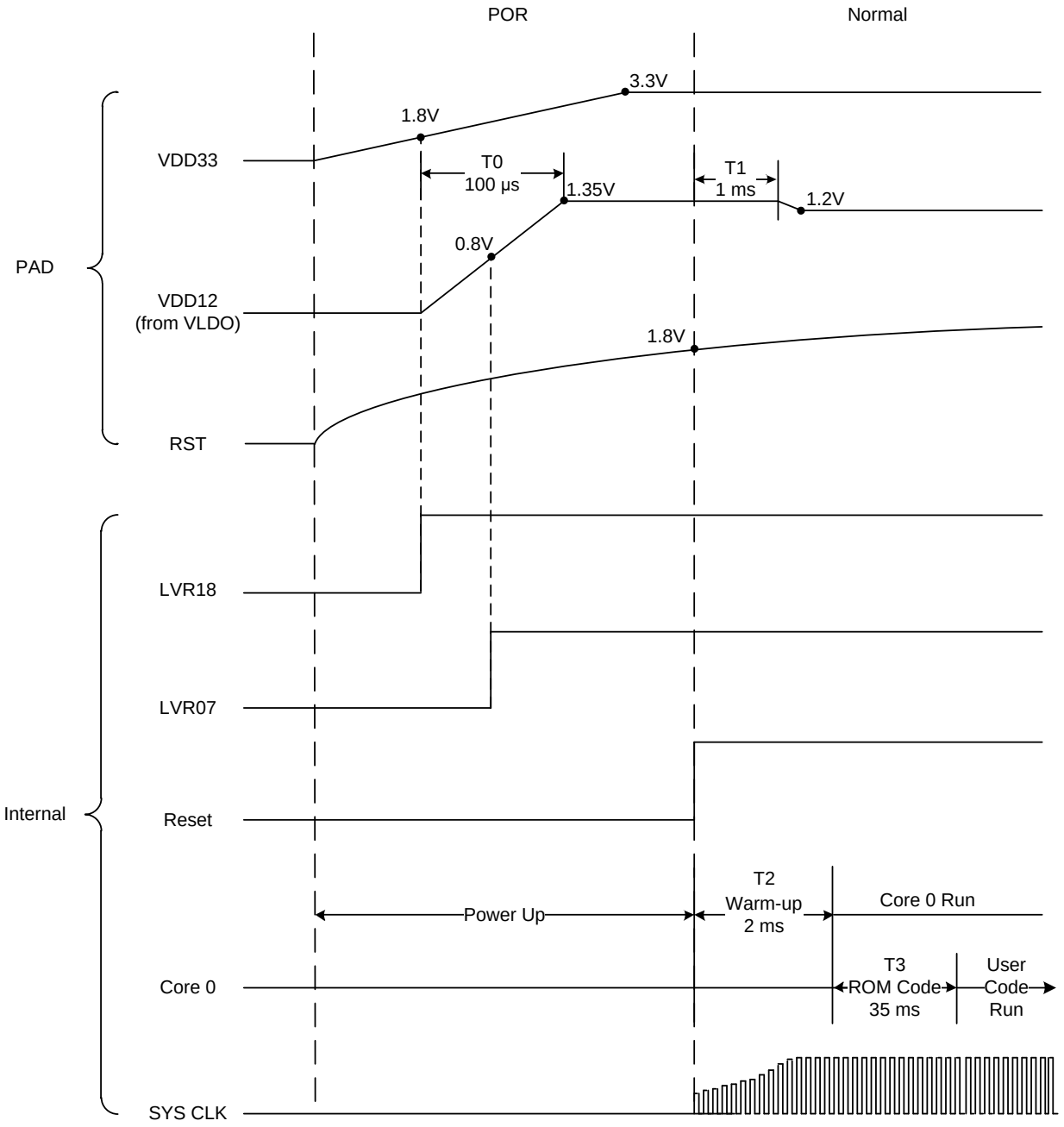


Figure 9–1 Power-up Sequence

Designs of the SNC7352x series must comply with the power-up sequence guidelines below to ensure reliable operation of the device.

Requirements:
1. VDD12 must be over 1.2V before M3 enters T1 state.
2. VDD33 must be over 1.8V before RST reaches 1.8V.

9.4.2 Deep Power-down (DPD) and Wakeup (WKP) Sequence

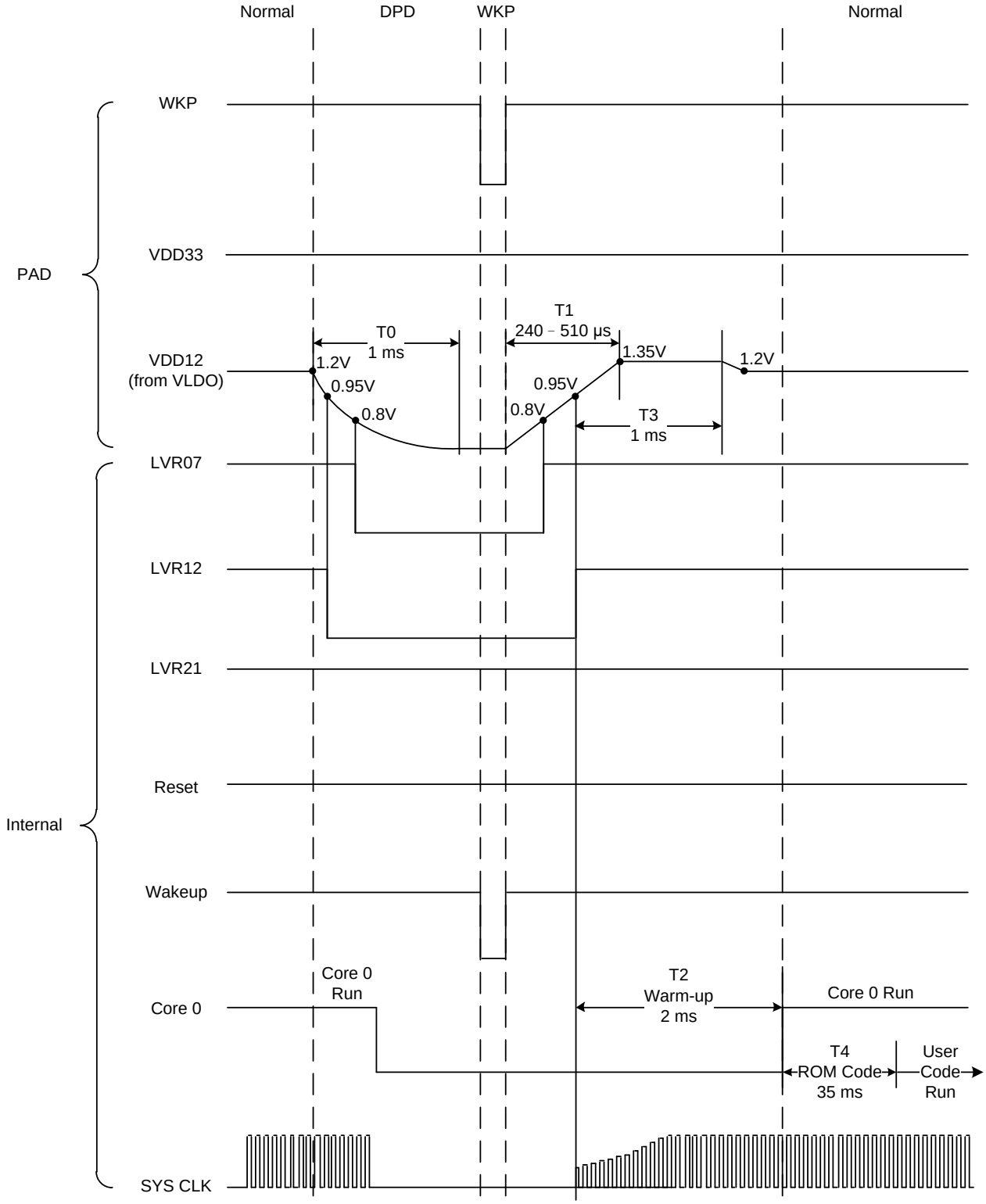


Figure 9–2 Deep Power-down and Wakeup Sequence

Requirement: The WKP signal must return to high before VDD12 enters T1 state.

10 Mechanical Data

10.1 Thermal Data

The permissible operating temperature range for the bearing is 0 °C to 85 °C.

10.2 Package Information

10.2.1 Nomenclature

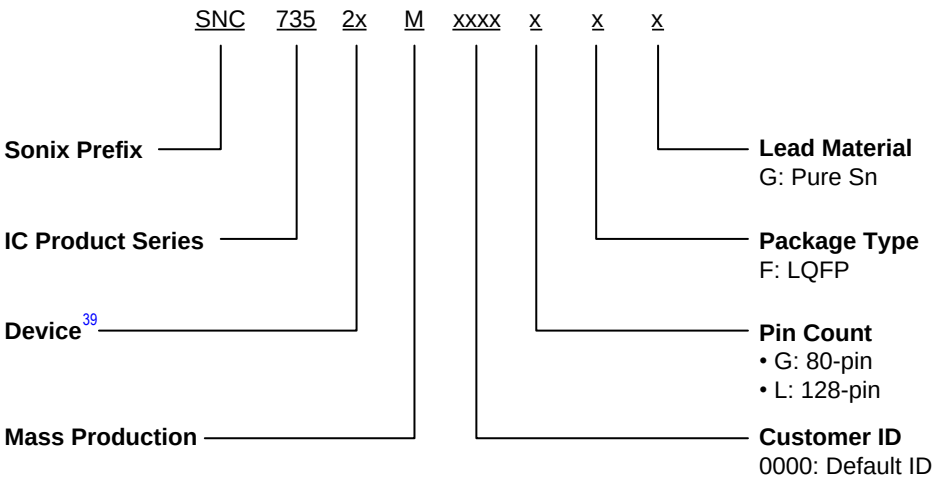


Figure 10–1 Nomenclature

[39] For details, refer to 2 Device Comparison.

10.2.2 Marking

The figure below is an example of the marking. Contents such as the product ID or symbol may vary according to different packages.

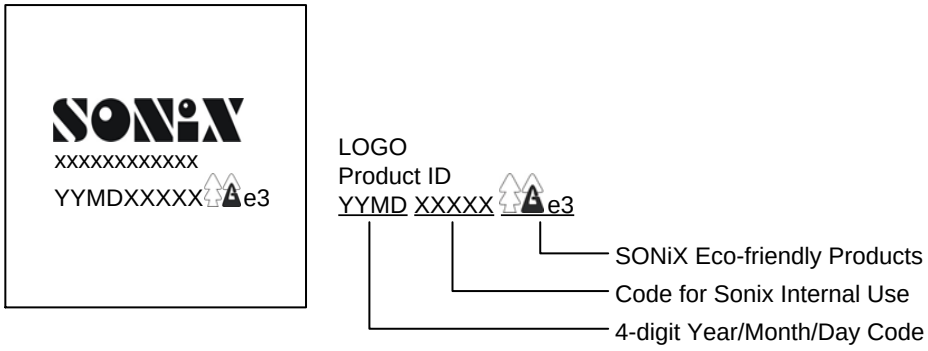
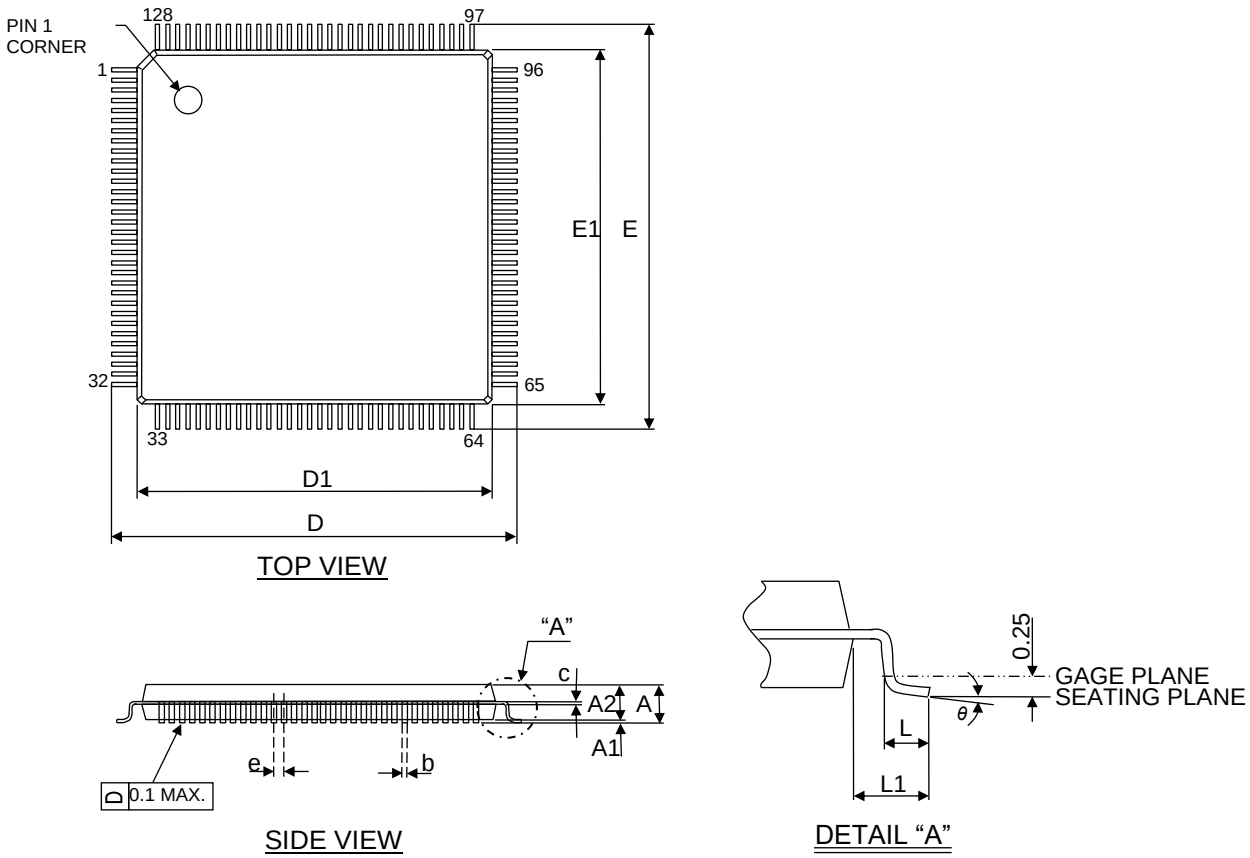


Figure 10–2 Example of Device Marking

10.2.3 Package Dimensions

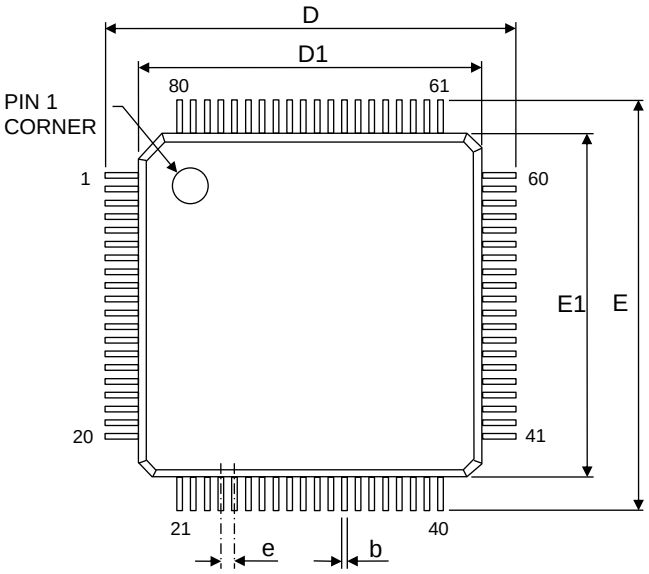
I. LQFP128L (14 x 14 x 1.4 mm/Pitch: 0.4)



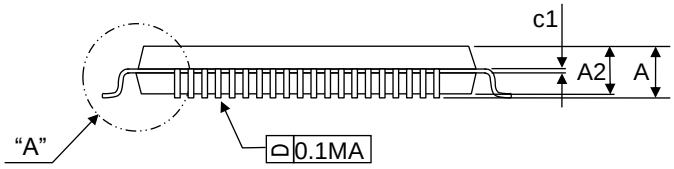
Symbols	Dimension in mm[40]			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.15	0.002	–	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b[41]	0.13	0.18	0.23	0.005	0.007	0.009
c	0.09	–	0.20	0.004	–	0.008
D	16.00 BSC			0.630 BSC		
D1[42]	14.00 BSC			0.551 BSC		
E	16.00 BSC			0.630 BSC		
E1[42]	14.00 BSC			0.551 BSC		
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
θ	0˚	3.5˚	7˚	0˚	3.5˚	7˚

[40] Controlling dimension: millimeter (mm)
[41] Dimension b does not include dambar protrusion.
[42] Dimension D1 and E1 do not include mold protrusion.

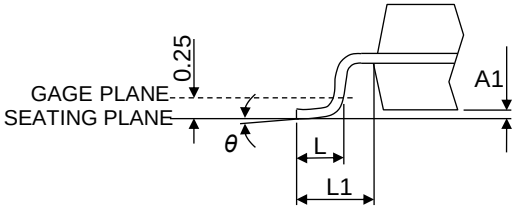
II. LQFP80L (10 x 10 x 1.4 mm/Pitch: 0.4)



TOP VIEW



SIDE VIEW



DETAIL "A"

Symbols	Dimension in mm[43]			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.20	0.002	–	0.008
A2	1.35	1.40	1.45	0.053	0.055	0.057
b[44]	0.13	0.18	0.23	0.005	0.007	0.009
c1	0.09	–	0.18	0.004	–	0.007
D	12 BSC			0.472 BSC		
D1[45]	10 BSC			0.394 BSC		
e	0.4 BSC			0.016 BSC		
E	12 BSC			0.472 BSC		
E1[45]	10 BSC			0.394 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.0 REF			0.039 REF		
θ	0°	3.5°	7°	0°	3.5°	7°

[43] Controlling dimension: millimeter (mm)
[44] Dimension "b" does not include dambar protrusion.
[45] Dimensions "D1" and "E1" do not include mold protrusion.

10.3 Packing Appearance and Storage Information

10.3.1 Packing Quantity

Table 10–1 Packing Quantity Information

Type	Pin Count	Carry Type	Package Size	IC Q'ty per Tube or Tray or Reel	Tube or Tray or Reel Q'ty per Inner Box	Total Q'ty in One Inner Box	Inner Box Q'ty per Carton	IC Q'ty per Carton
LQFP	128	Tray	14 x 14	90	10	900	6	5400
LQFP	80	Tray	10 x 10	160	10	1600	6	9600

10.3.2 Packing Dimension

Table 10–2 Inner Box/Carton Dimension for LQFP128L/LQFP80L

Inner Box/Carton	Dimension in mm
Inner box	360 x 152 x 90
Carton	470 x 370 x 210
Carton (optional)	380 x 340 x 300

10.3.3 Temperature and Humidity Environmental Control Requirements in Storage

Table 10–3 Storage Condition

Control Requirement	Specification
Temperature (°C)	24 ± 6
Humidity (% RH)	60 ± 20

10.3.4 Shelf-life

1. The shelf life for unopened vacuum pack products is four years after the date on the label.
2. Once the packing is opened the product should be conducted SMT process within 168 hours and environmental control is under ≤ 30°C / 60% RH.
3. If the product has been exposed to the room environment for more than 168 hours, it should be baked in an oven at 125°C for 10 hours and vacuum packed.

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